EE 330
Lecture 36

High Frequency Operation of Amplifiers

Digital Circuit Design

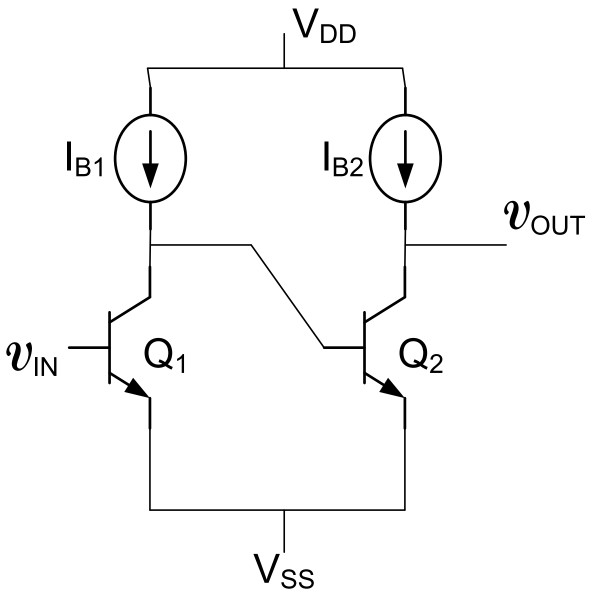
Hierarchical Design

Fall 2024 Exam Schedule

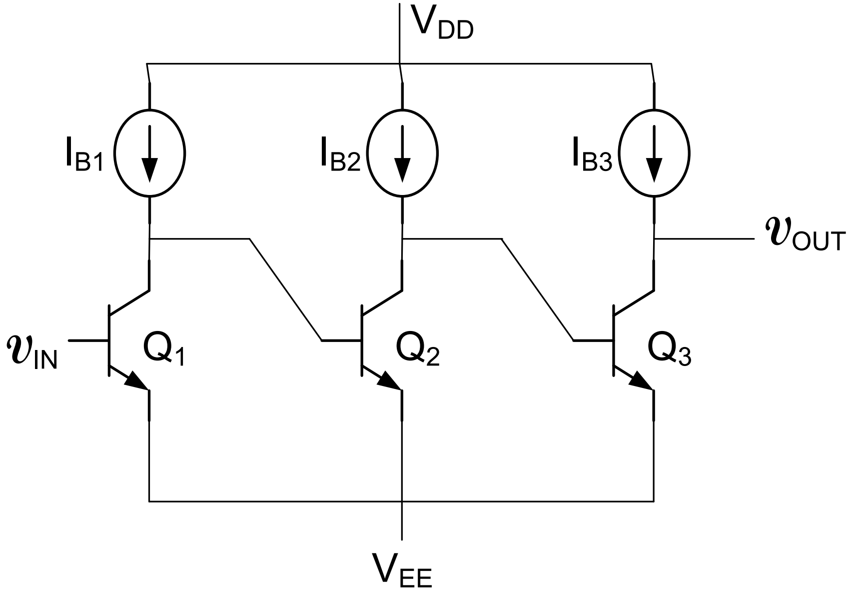
Exam 1	Friday	Sept 27
Exam 2	Friday	October 25
Exam 3	Friday	Nov 22
Final Exam	Monday	Dec 16 12:00 - 2:00 PM

Review from Last Lecture

Cascade Configurations



Two-stage CE Cascade

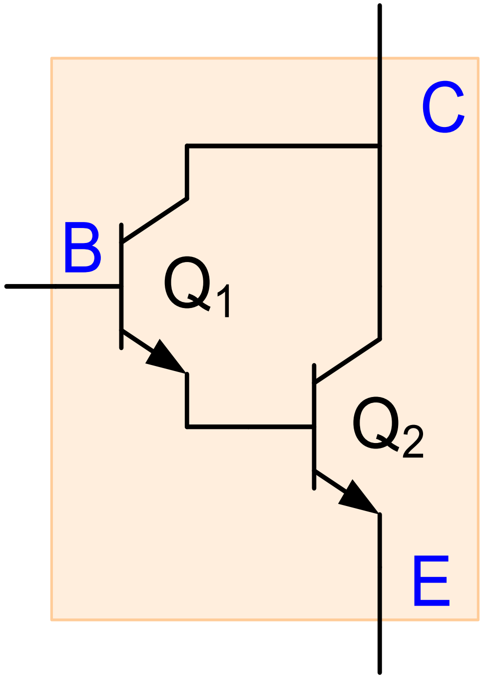


Three-stage CE Cascade

- **Large gains can be obtained by cascading**
- **Gains are multiplicative (when loading is included)**
- **Large gains used to build “Op Amps” and feedback used to control gain value**
- **Some attention is needed for biasing but it is manageable**
- **Minor variant of the two-stage cascade often used to build Op Amps**
- **Compensation of two-stage cascade needed if feedback is applied to maintain stability**
- **For many years three or more stages were seldom cascaded because of challenges in compensation to maintain stability though recently some industrial adoptions**

Review from Last Lecture

Other Basic Configurations



Darlington Configuration

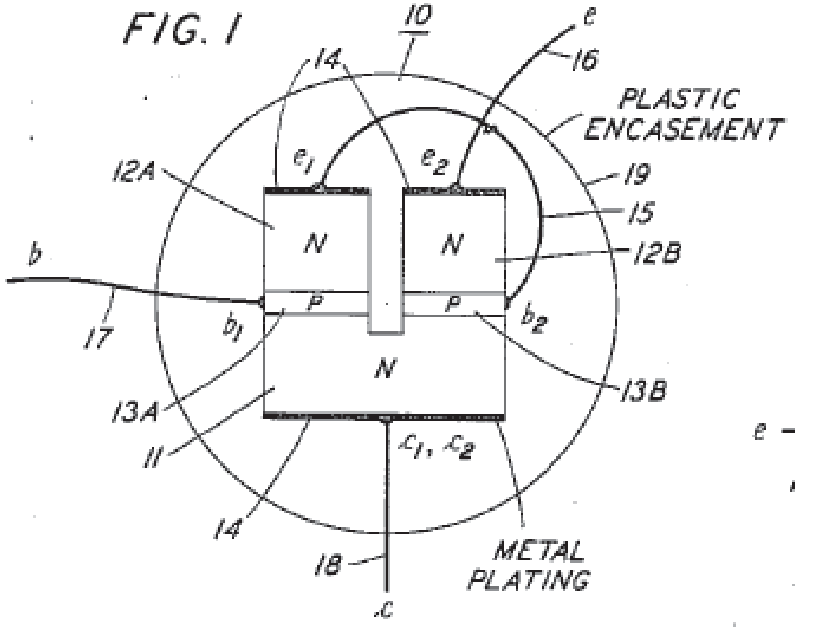


FIG. I

S. DARLINGTON 2,663,806

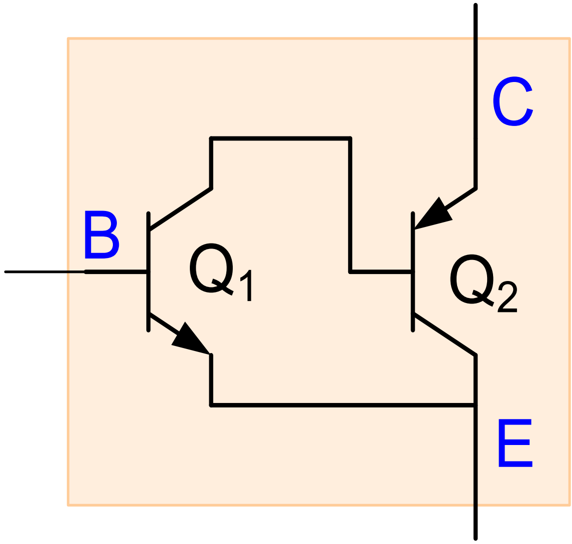
SEMICONDUCTOR SIGNAL TRANSLATING DEVICE

Filed May 9, 1952

- **Current gain is approximately β^2**
- **Two diode drop between B_{eff} and E_{eff}**

Review from Last Lecture

Other Basic Configurations



Sziklai Pair

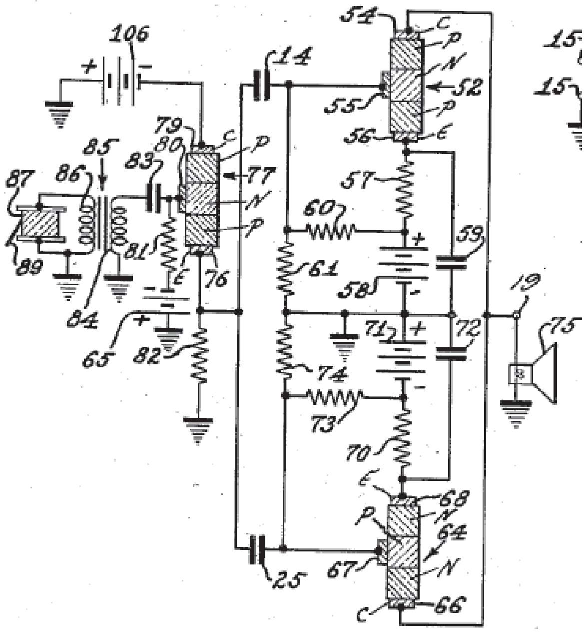


FIG. 3.

May 7, 1957 G. C. SZIKLAI 2,791,644

PUSH-PULL AMPLIFIER WITH COMPLEMENTARY TYPE TRANSISTORS

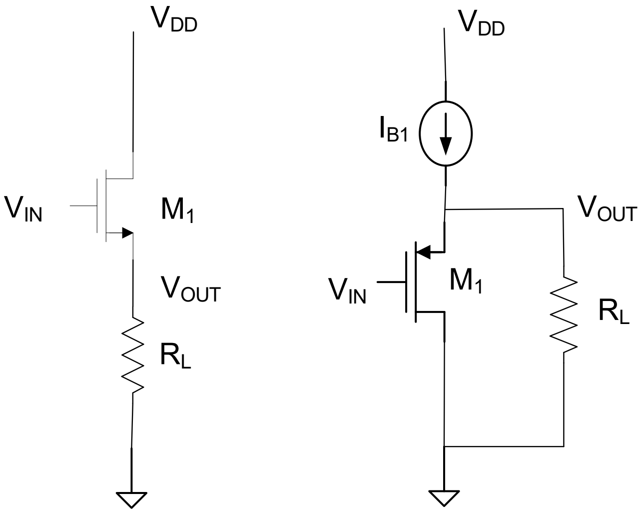
Filed Nov. 7, 1952

- **Gain similar to that of Darlington Pair**
- **Current gain is approximately $\beta_n \beta_p$**
- **Current gain will not be as large when $\beta_p < \beta_n$**
- **Only one diode drop between B_{eff} and E_{eff}**

Review from Last Lecture

Other Basic Configurations

Buffer



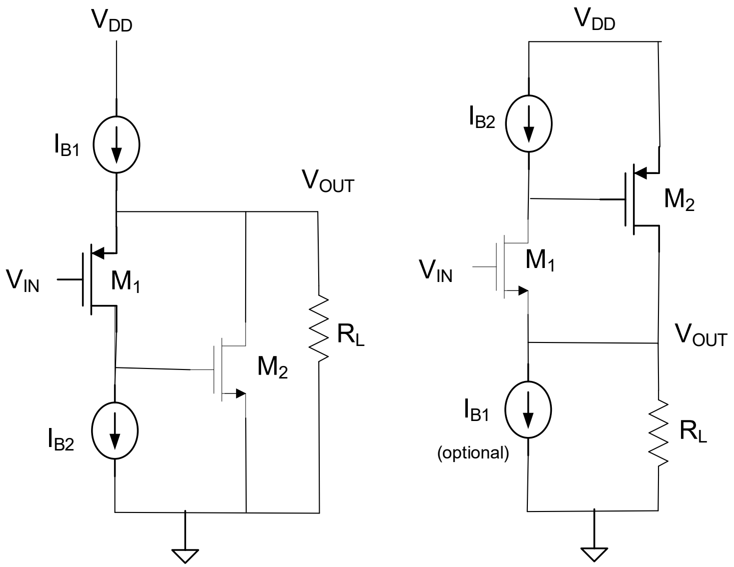
Ideally $V_{OUT}=V_{IN}$

Assume load terminated on gnd

Current through M_1 changes with V_{IN}

Voltage shift varies with V_{IN} in buffer

Super Buffer



Ideally $V_{OUT}=V_{IN}$

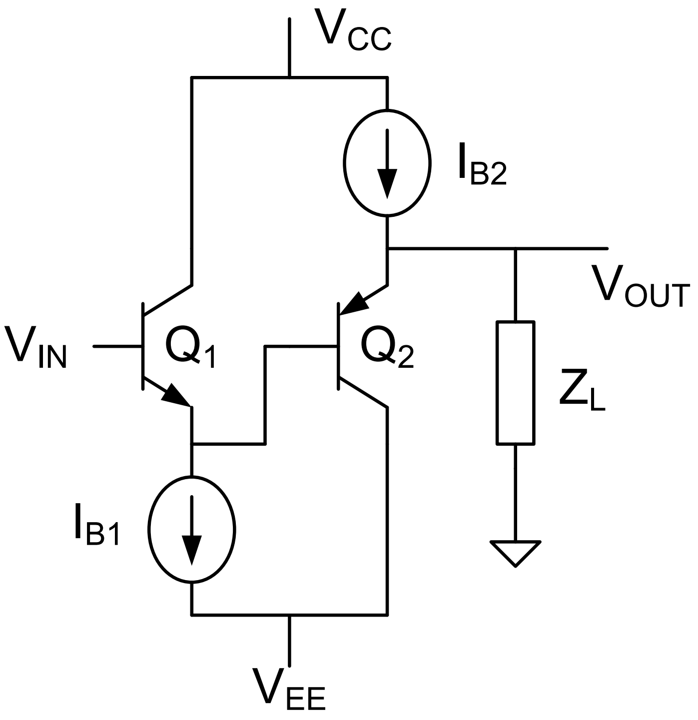
Assume load terminated on gnd

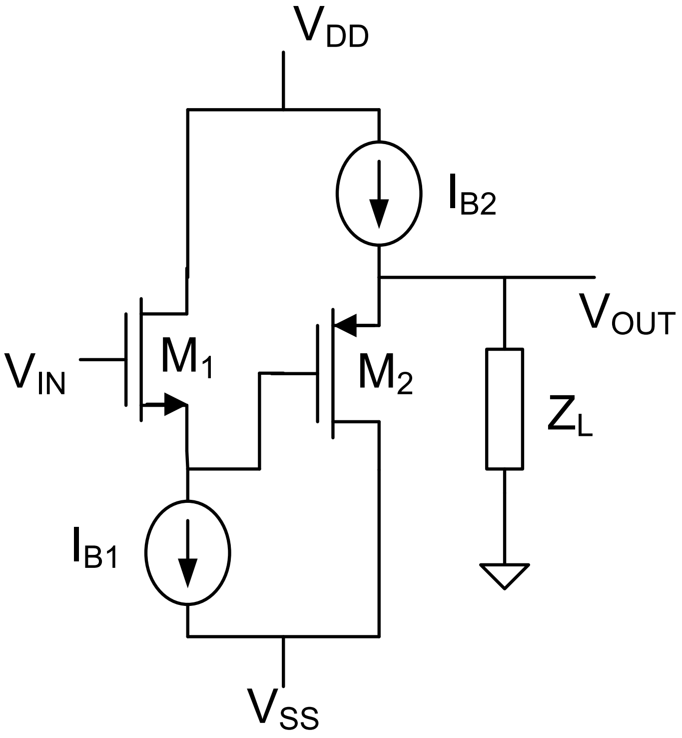
Current through shift transistor is constant for Super Buffer as V_{IN} changes so voltage shift does not change with V_{IN}

Same nominal voltage shift as buffer

Other Basic Configurations

Low offset buffers



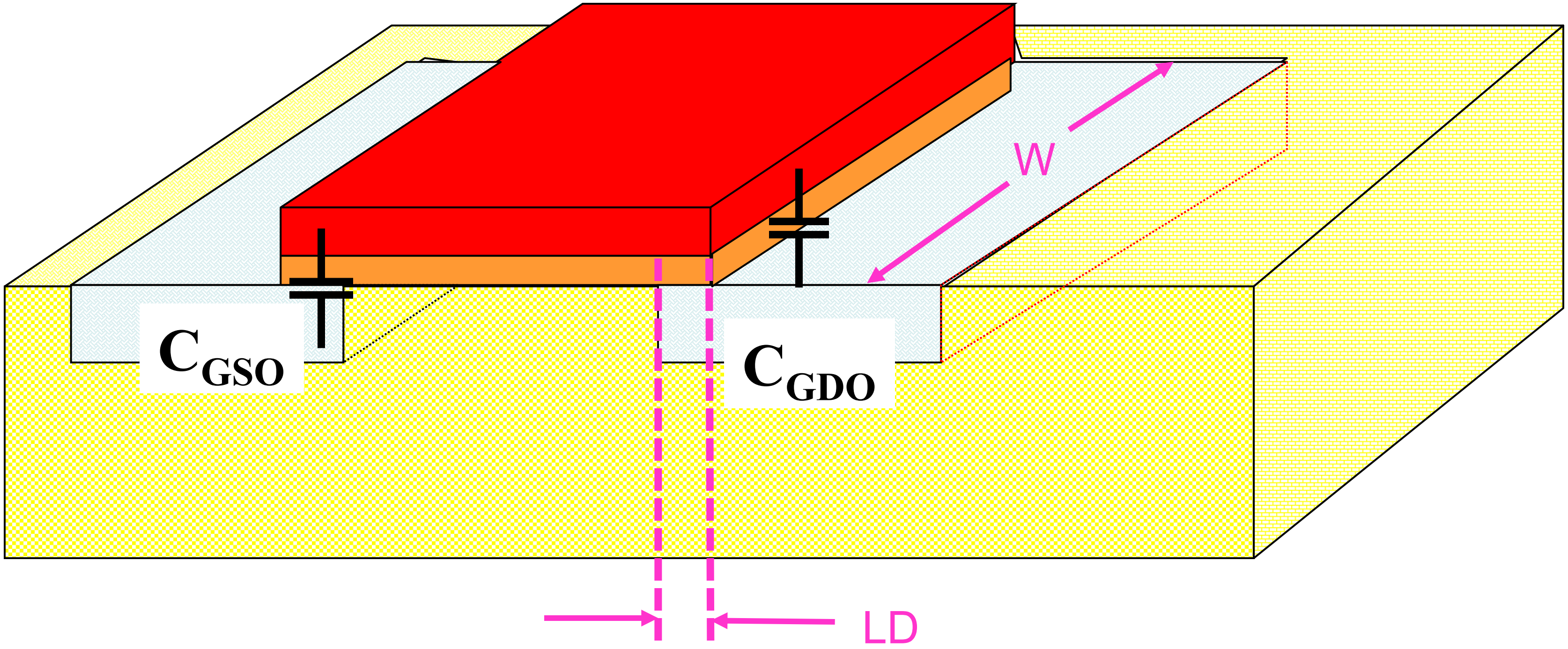


- **Actually a CC-CC or a CD-CD cascade**
- **Significant drop in offset between input and output**
- **Biasing with DC current sources**
- **Can Add Super Buffer to Output**

Material Not Covered From Last Lecture
Start Here

Parasitic Capacitors in MOSFET

Fixed Capacitors – Fixed Geometry

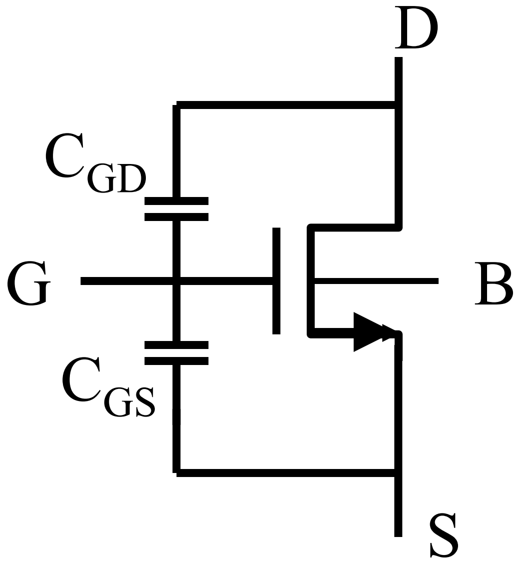


Overlap Capacitors: C_{GDO}, C_{GSO}

Cap Density: C_{OX}

L_D: lateral diffusion

Parasitic Capacitance Summary (partial)



	Cutoff	Ohmic	Saturation
C_{GSO}	$C_{ox}WL_D$	$C_{ox}WL_D$	$C_{ox}WL_D$
C_{GDO}	$C_{ox}WL_D$	$C_{ox}WL_D$	$C_{ox}WL_D$

L_D is a model parameter

Overlap Capacitance Model Parameters

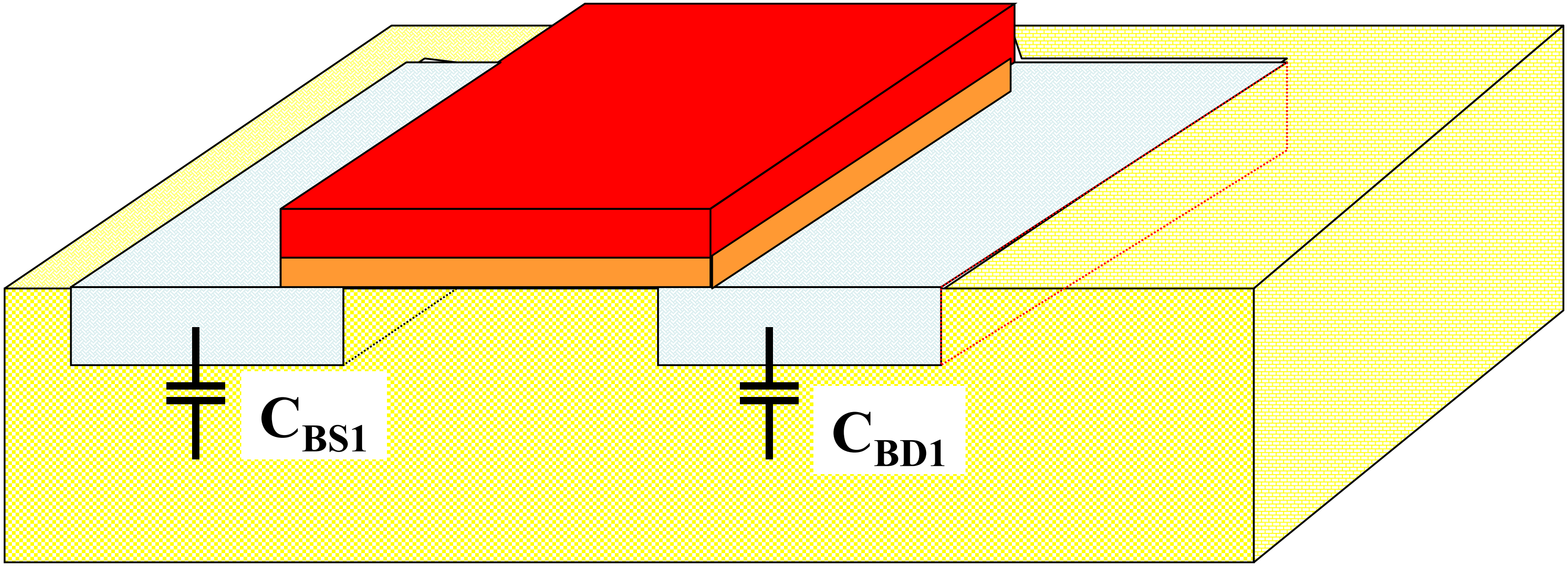
```
CAPACITANCE PARAMETERS N+ P+ POLY  M1 M2 M3 M4 M5 M6 R_W  D_N_W M5P N_W  UNITS
 Area (substrate)     942 1163 106 34 14  9  6  5  3         123    125 aF/um^2
 Area (N+active)              8484 55 20 13 11  9  8                    aF/um^2
 Area (P+active)              8232                                      aF/um^2
 Area (poly)                       66 17 10  7  5  4                    aF/um^2
 Area (metal1)                        37 14  9  6  5                    aF/um^2
 Area (metal2)                           35 14  9  6                    aF/um^2
 Area (metal3)                              37 14  9                    aF/um^2
 Area (metal4)                                 36 14                    aF/um^2
 Area (metal5)                                    34              984   aF/um^2
 Area (r well)         920                                              aF/um^2
 Area (d well)                                          582             aF/um^2
 Area (no well)        137                                              aF/um^2
 Fringe (substrate)    212  235    41 35 29 21 14                        aF/um
 Fringe (poly)                     70 39 29 23 20 17                     aF/um
 Fringe (metal1)                      52 34    22 19                     aF/um
 Fringe (metal2)                         48 35 27 22                     aF/um
 Fringe (metal3)                            53 34 27                     aF/um
 Fringe (metal4)                               58 35                     aF/um
 Fringe (metal5)                                  55                     aF/um
 Overlap (N+active)             895                                      aF/um
 Overlap (P+active)             737                                      aF/um
```

Types of Capacitors in MOSFETs

1. Fixed Capacitors
    a. Fixed Geometry
    b. Junction
2. Operating Region Dependent

Parasitic Capacitors in MOSFET

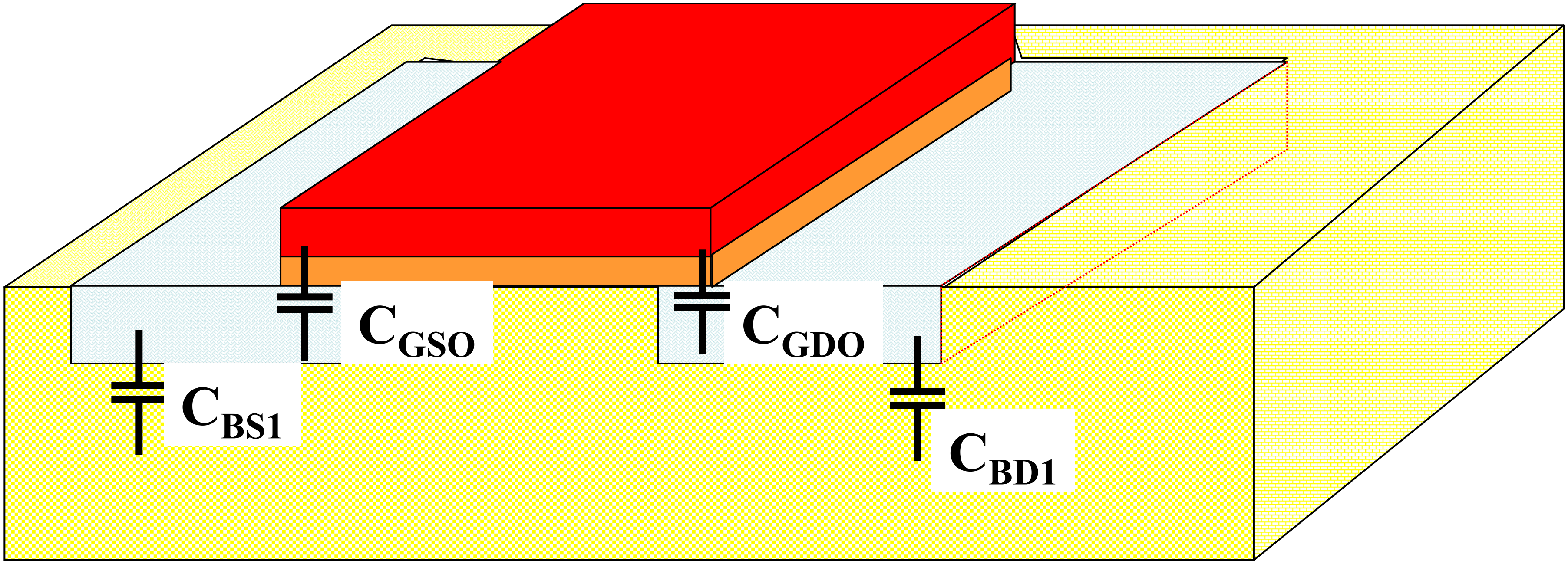
Fixed Capacitors- Junction



Junction Capacitors: C_{BS1}, C_{BD1}

Parasitic Capacitors in MOSFET

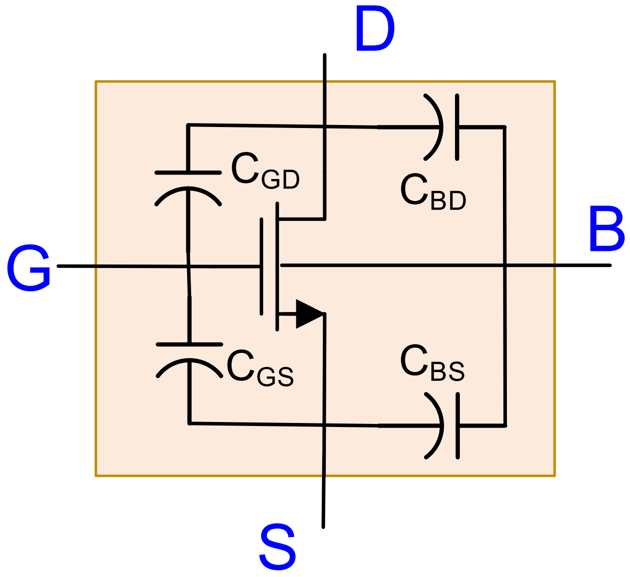
- Fixed Capacitors



Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Fixed Parasitic Capacitance Summary



C_{BOT} and C_{SW} are model parameters

	Cutoff	**Ohmic**	**Saturation**
$\mathbf{C_{GSO}}$	$C_{ox}WL_D$	$C_{ox}WL_D$	$C_{ox}WL_D$
$\mathbf{C_{GDO}}$	$C_{ox}WL_D$	$C_{ox}WL_D$	$C_{ox}WL_D$
$\mathbf{C_{BG}}$			
$\mathbf{C_{BS}}$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
$\mathbf{C_{BD}}$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

C_{BOT} and C_{SW} model parameters

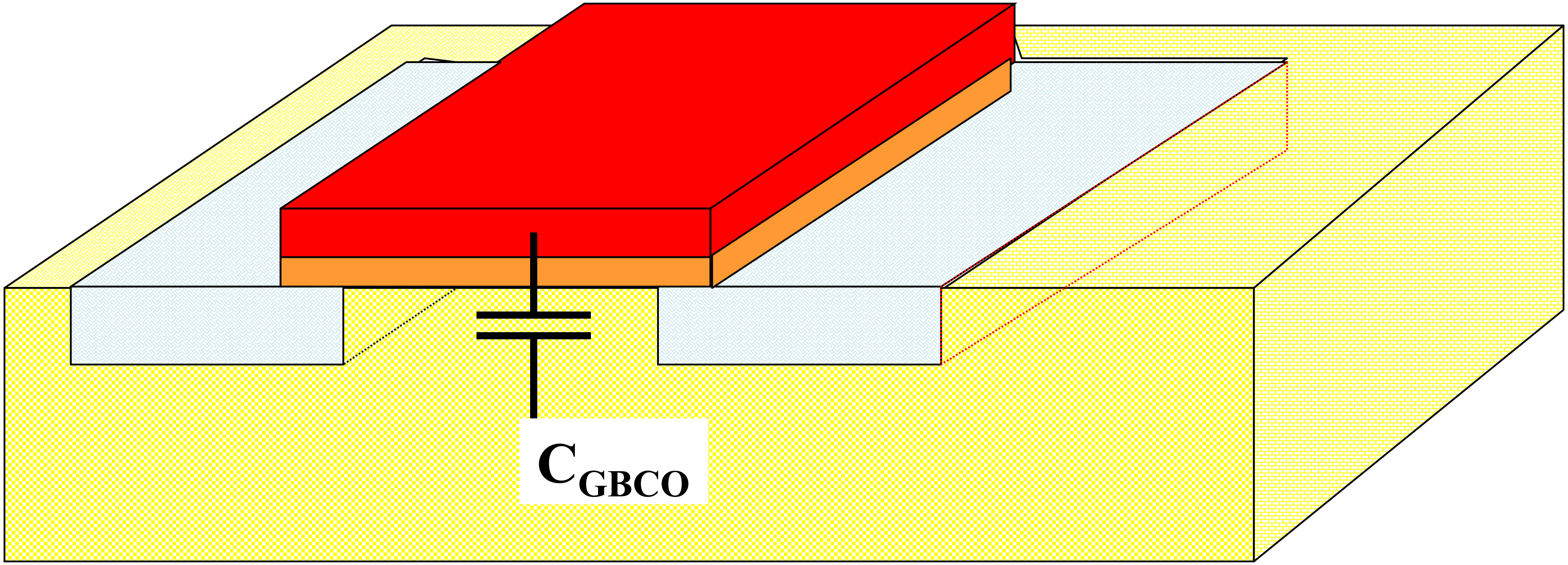
```
CAPACITANCE PARAMETERS N+ P+ POLY  M1 M2 M3 M4 M5 M6 R_W  D_N_W M5P N_W  UNITS
 Area (substrate)     942 1163 106 34 14  9  6  5  3         123    125 aF/um^2
 Area (N+active)              8484 55 20 13 11  9  8                    aF/um^2
 Area (P+active)              8232                                      aF/um^2
 Area (poly)                       66 17 10  7  5  4                    aF/um^2
 Area (metal1)                        37 14  9  6  5                    aF/um^2
 Area (metal2)                           35 14  9  6                    aF/um^2
 Area (metal3)                              37 14  9                    aF/um^2
 Area (metal4)                                 36 14                    aF/um^2
 Area (metal5)                                    34              984   aF/um^2
 Area (r well)         920                                              aF/um^2
 Area (d well)                                        582               aF/um^2
 Area (no well)        137                                              aF/um^2
 Fringe (substrate)    212  235    41 35 29 21 14                        aF/um
 Fringe (poly)                     70 39 29 23 20 17                     aF/um
 Fringe (metal1)                      52 34    22 19                     aF/um
 Fringe (metal2)                         48 35 27 22                     aF/um
 Fringe (metal3)                            53 34 27                     aF/um
 Fringe (metal4)                               58 35                     aF/um
 Fringe (metal5)                                  55                     aF/um
 Overlap (N+active)             895                                      aF/um
 Overlap (P+active)             737                                      aF/um
```

Types of Capacitors in MOSFETs

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction
2. Operating Region Dependent

Parasitic Capacitors in MOSFET

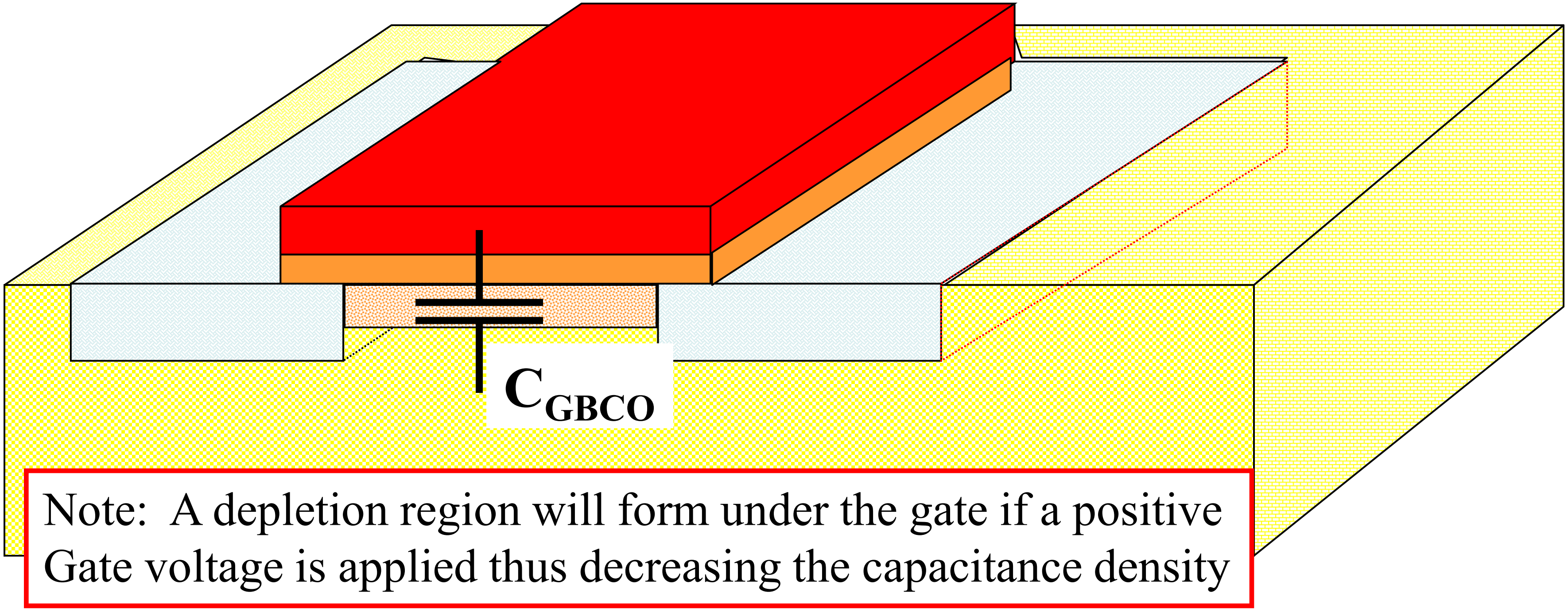
Operation Region Dependent -- Cutoff



Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Cutoff

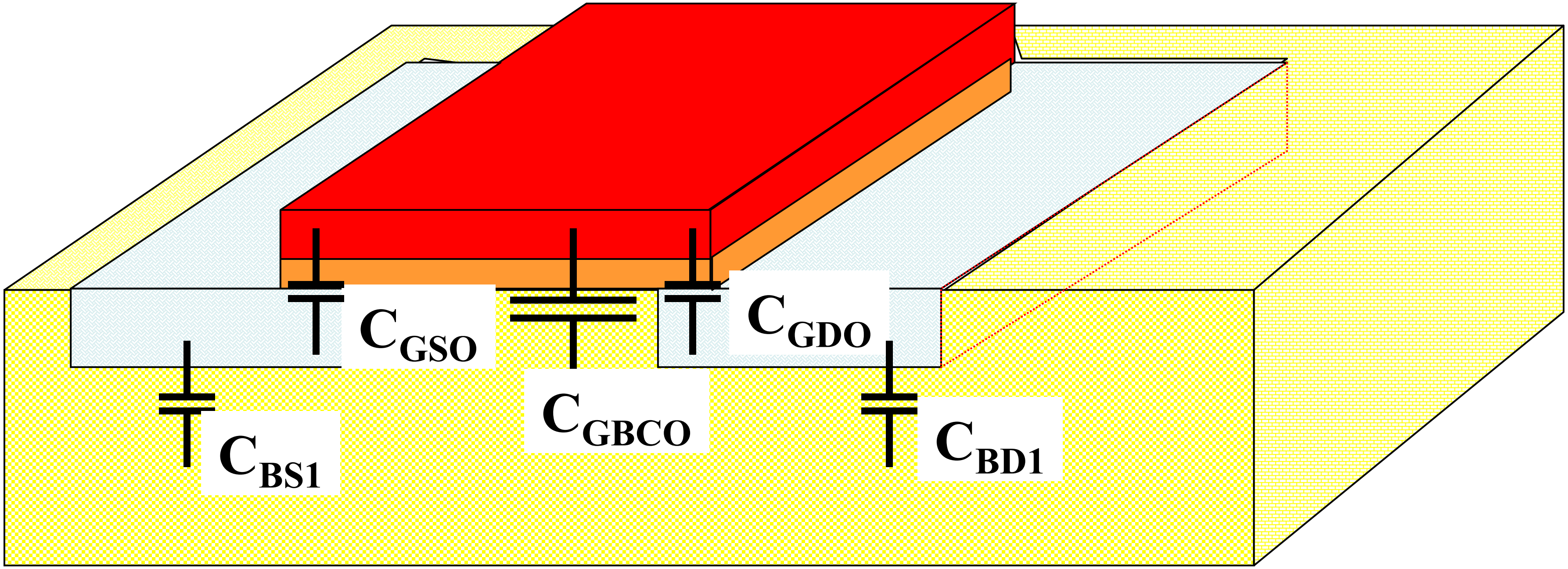


Note: A depletion region will form under the gate if a positive Gate voltage is applied thus decreasing the capacitance density

Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Cutoff

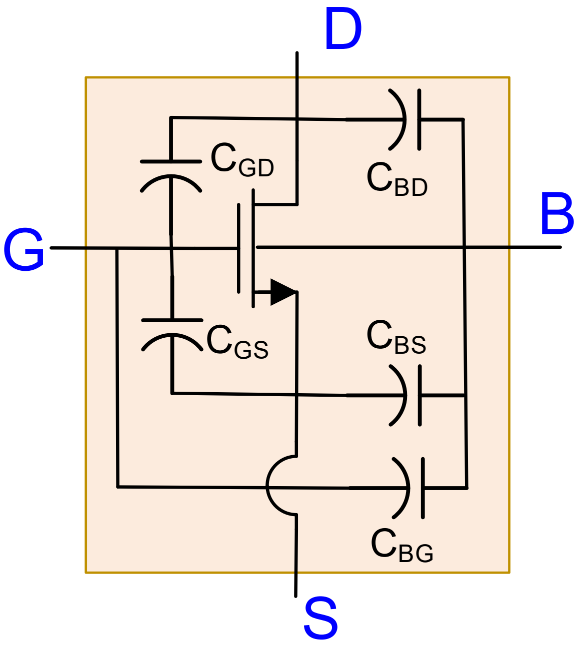


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Cutoff Capacitor: C_{GBCO}

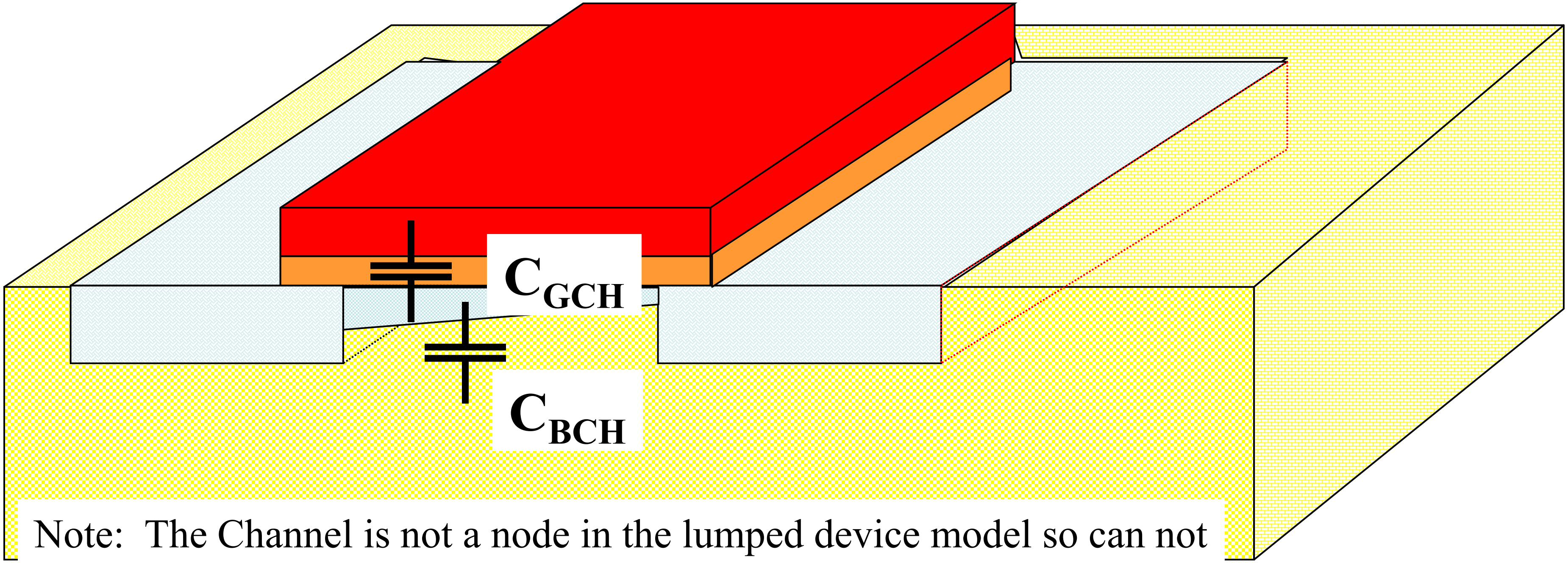
Parasitic Capacitance Summary



	Cutoff	**Ohmic**	**Saturation**
C_{GSO}	$C_{ox}WL_D$		
C_{GDO}	$C_{ox}WL_D$		
C_{BG}	$C_{ox}WL$ (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$		
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$		

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Ohmic



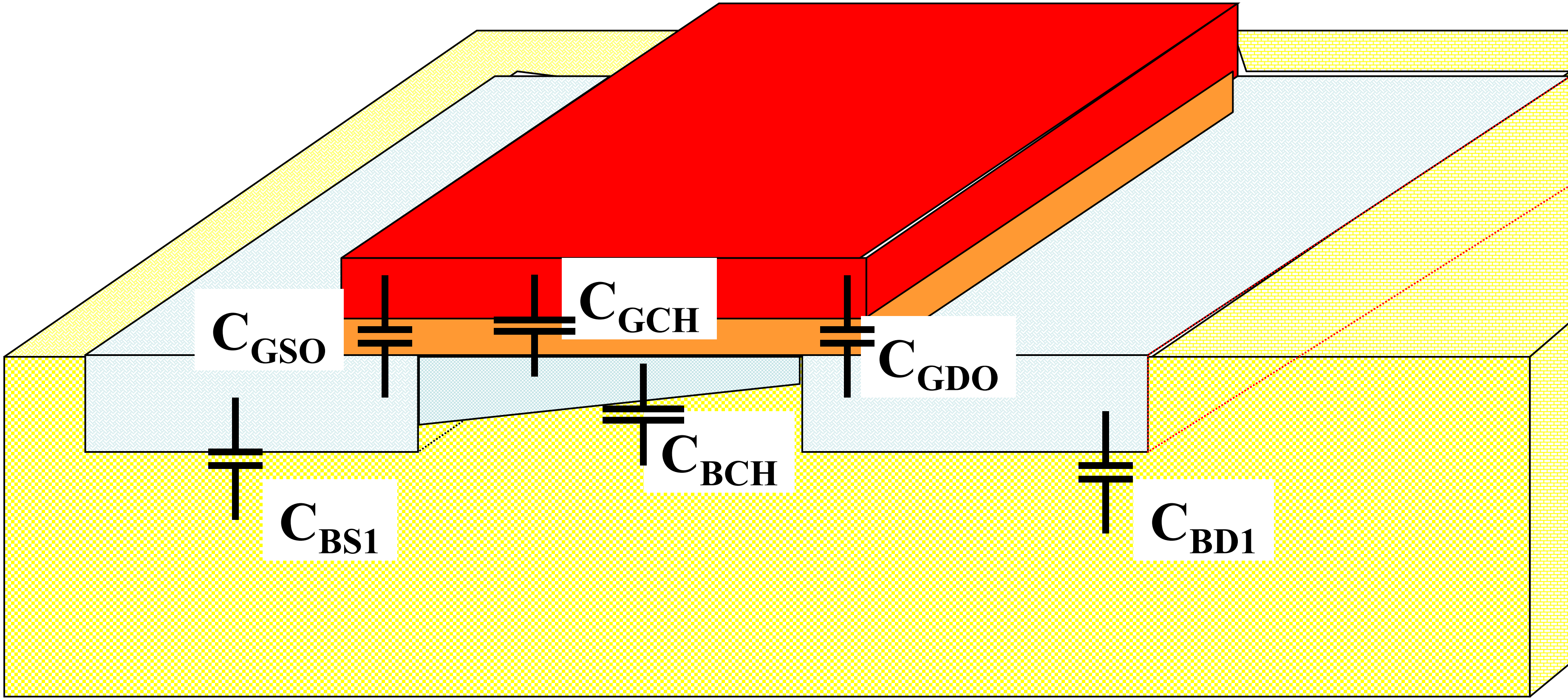
Note: The Channel is not a node in the lumped device model so can not directly include this distributed capacitance in existing models

Note: The distributed channel capacitance is usually lumped and split evenly between the source and drain nodes

Ohmic Capacitor: C_{GCH} , C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Ohmic

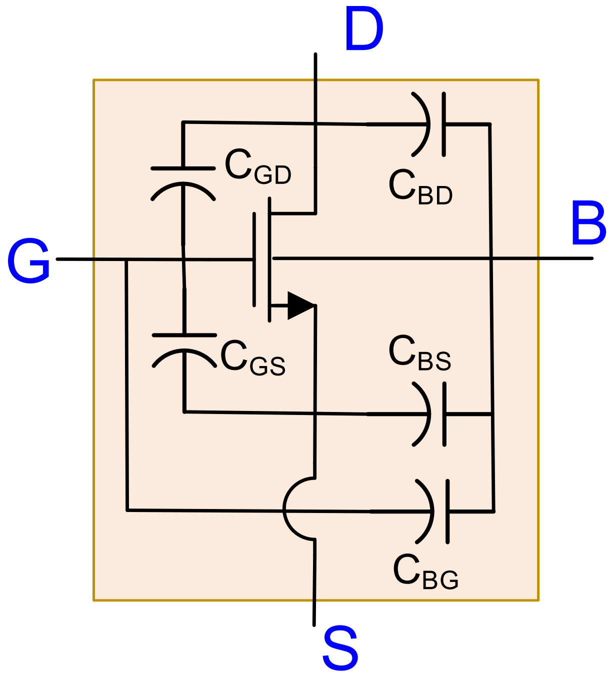


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Ohmic Capacitor: C_{GCH} , C_{BCH}

Parasitic Capacitance Summary

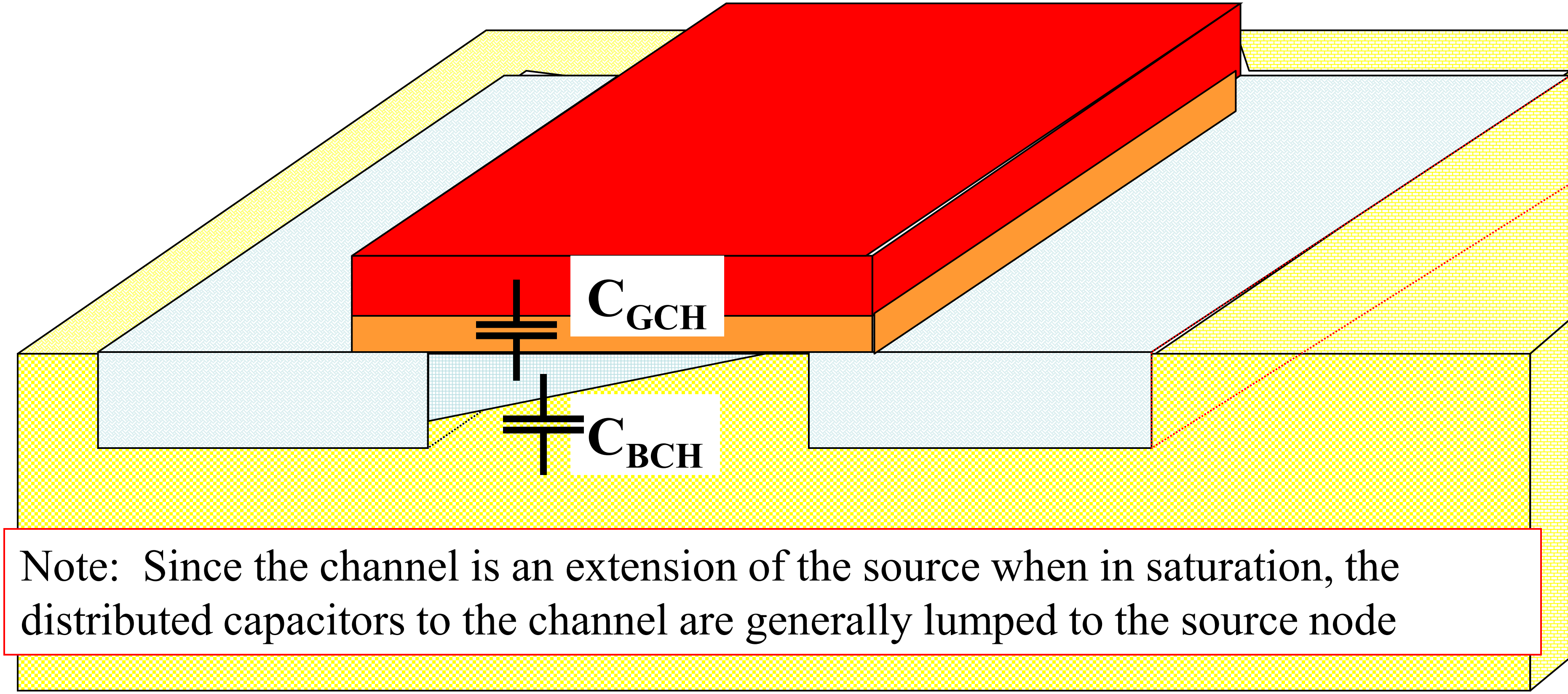


Lumped C_{GC} and C_{BC} to analytically avoid dealing with distributed capacitance

	Cutoff	**Ohmic**	**Saturation**
$\mathbf{C_{GS}}$	$C_{ox}WL_D$	$0.5C_{ox}WL$	
$\mathbf{C_{GD}}$	$C_{ox}WL_D$	$0.5C_{ox}WL$	
$\mathbf{C_{BG}}$	$C_{ox}WL$ (or less)	0	
$\mathbf{C_{BS}}$	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	
$\mathbf{C_{BD}}$	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Saturation

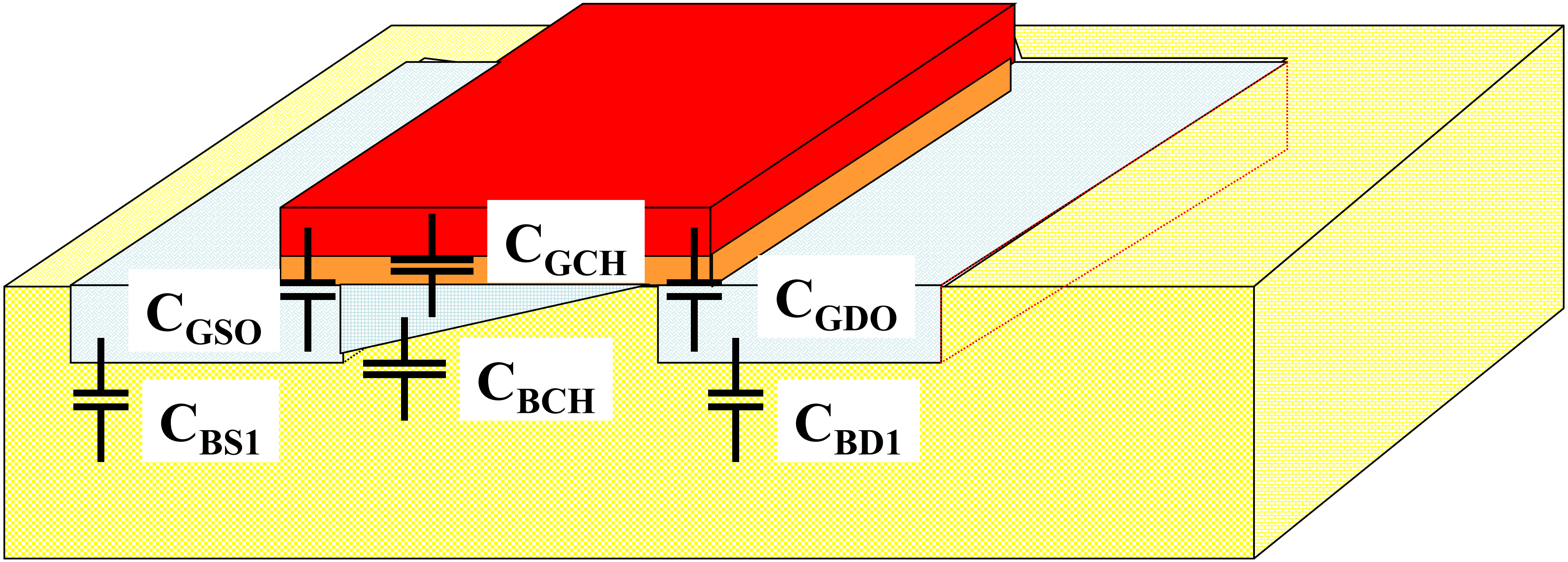


Note: Since the channel is an extension of the source when in saturation, the distributed capacitors to the channel are generally lumped to the source node

Saturation Capacitors: C_{GCH} , C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed --Saturation



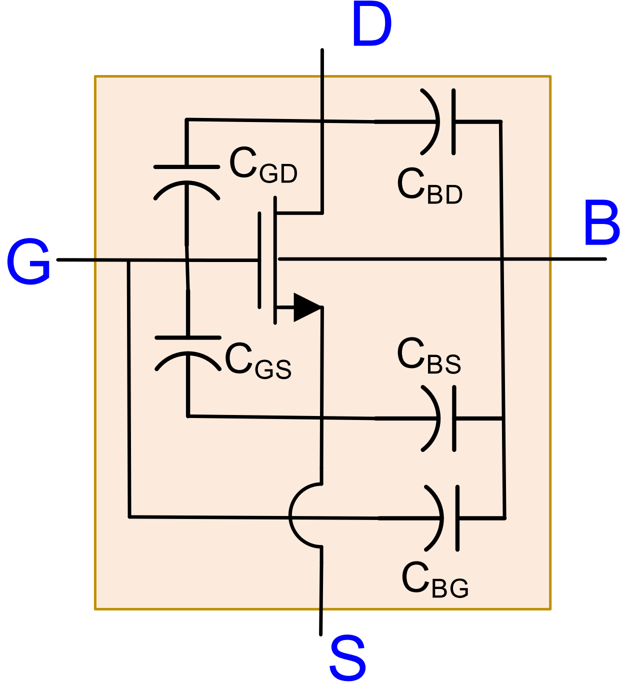
Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Saturation Capacitors: C_{GCH} , C_{BCH}

- 2/3 $C_{OX}WL$ is often attributed to C_{GCH} to account for LD and saturation
- This approximation is reasonable for minimum-length devices but not so good for longer devices

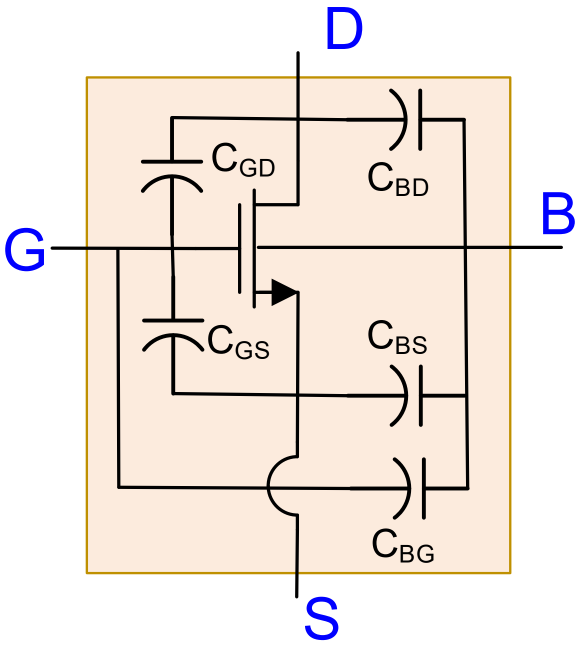
Parasitic Capacitance Summary



Lumped C_{GC} and C_{BC} to analytically avoid dealing with distributed capacitance

	Cutoff	**Ohmic**	**Saturation**
C_{GS}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

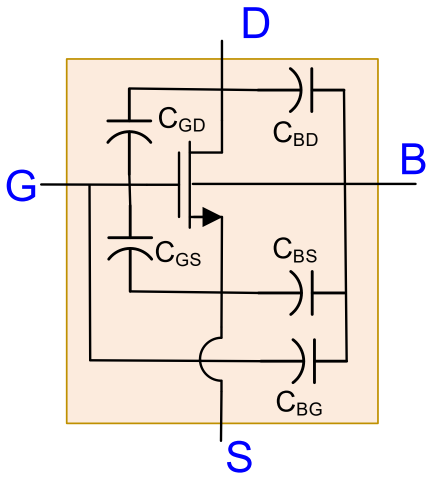
Parasitic Capacitance Summary



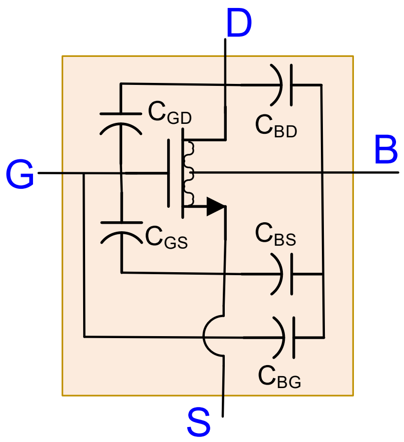
	Cutoff	**Ohmic**	**Saturation**
$\mathbf{C_{GS}}$	$C_{OX}WL_D$	$0.5C_{OX}WL$	$C_{OX}WL_D+(2/3)C_{OX}WL$
$\mathbf{C_{GD}}$	$C_{OX}WL_D$	$0.5C_{OX}WL$	$C_{OX}WL_D$
$\mathbf{C_{BG}}$	$C_{OX}WL$ (or less)	0	0
$\mathbf{C_{BS}}$	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
$\mathbf{C_{BD}}$	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Observe there is no C_{DS} in this model because does not physically exist

Parasitic Capacitance Summary

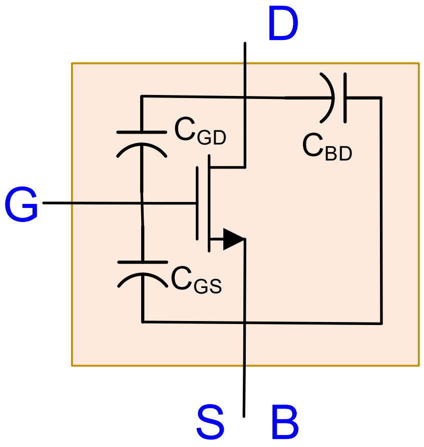


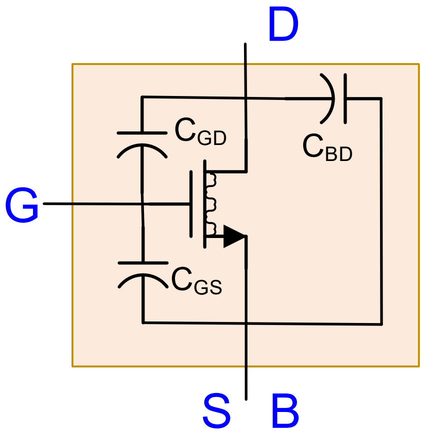
High Frequency Large Signal Model



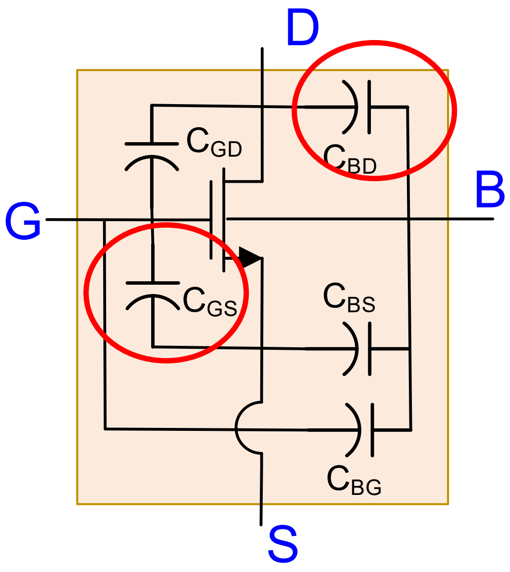
High Frequency Small Signal Model

Often V_{BS}=0 and C_{BG}=0, so simplifies to





Parasitic Capacitance Implications



The parasitic capacitances inherently introduce an upper limit on how fast either digital circuits or analog circuits can operate in a given process

Two parameters, f_{MAX} and f_T, (not defined yet) are two metric that are used to specify the fundamental speed limit in a semiconductor process

The dominant parasitic capacitances for most circuits are C_{GS} and C_{BD}

Material Not Covered From Last Lecture End Here

f_T and f_{MAX} for a semiconductor process

f_T is defined to be the frequency where the short-circuit current gain of a transistor drops to unity

f_{MAX} is defined to be the frequency where the power gain of the transistor drops to unity (related to the maximum frequency of oscillation in a process)

$$f_T \simeq \frac{3}{4\pi}\frac{\mu V_{EB}}{L_{min}^2} = \frac{3}{16\pi}\frac{\mu\left|V_{DD}-V_{TH}\right|}{\left(\lambda - LD\right)^2} \qquad (2\lambda = L_{min})$$

f_T strongly dependent on V_{EB}

for the ON 0.5u process

u_nC_{OX}=100uA/V^2
C_{OX}=2.4fF/u^2
λ=0.2u
LD=.05u
V_{THn}=0.8V

u_n=4E10$A\mu^2F^{-1}V^{-2}$
u_n=400$cm^2AF^{-1}V^{-2}$

At V_{EB}=1V, f_T=25GHz

Note: As feature sizes shrink with process nodes, $V_{EB\text{-}MAX}$ will typically drop linearly but L_{min} will drop quadratically thus f_T gets much larger in small feature processes

f_T and f_{MAX} for a semiconductor process

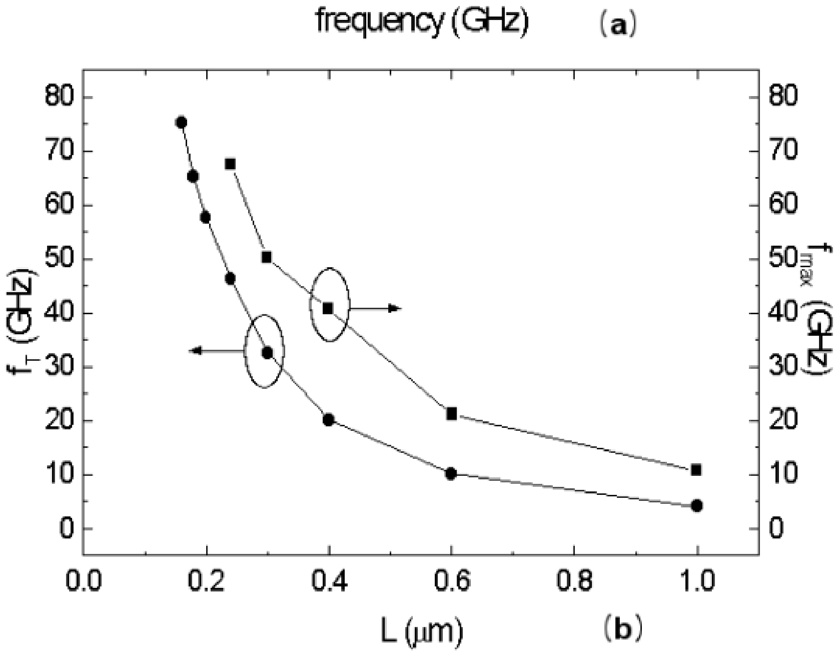
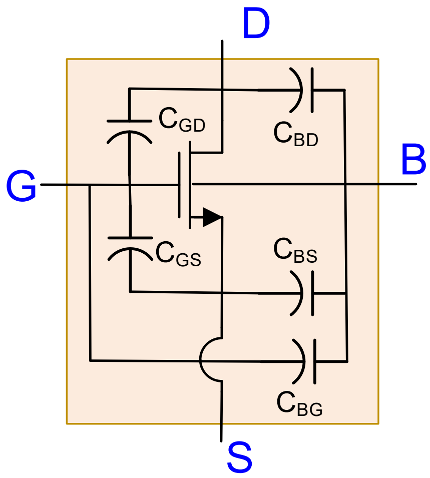


Fig. 7. (a) Maximum stable gain (MSG) and maximum available gain (MAG) for different channel lengths and (b) the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) as functions of the channel length.

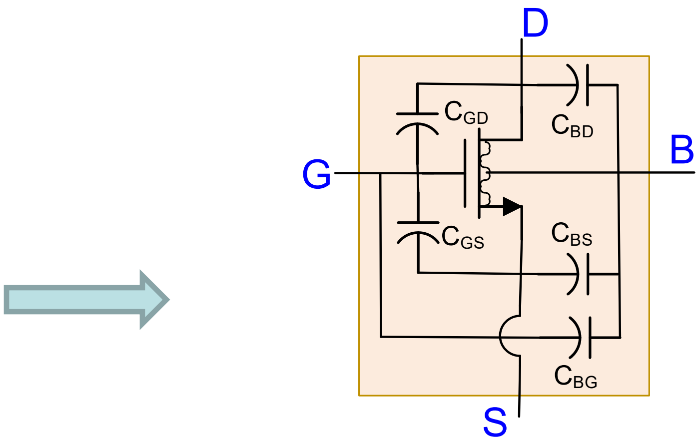
For 0.18u process, V_D=2V, V_G=1.2V

Journal of the Korean Physical Society, Vol. 40, No. 1, January 2002, pp. 45~48

Parasitic Capacitance Summary

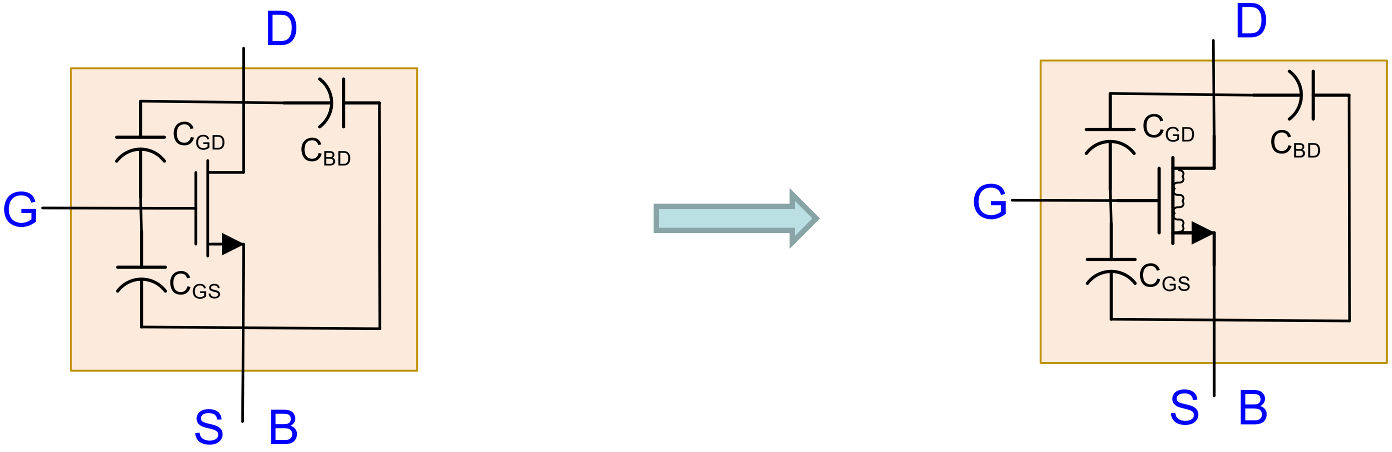


High Frequency Large Signal Model



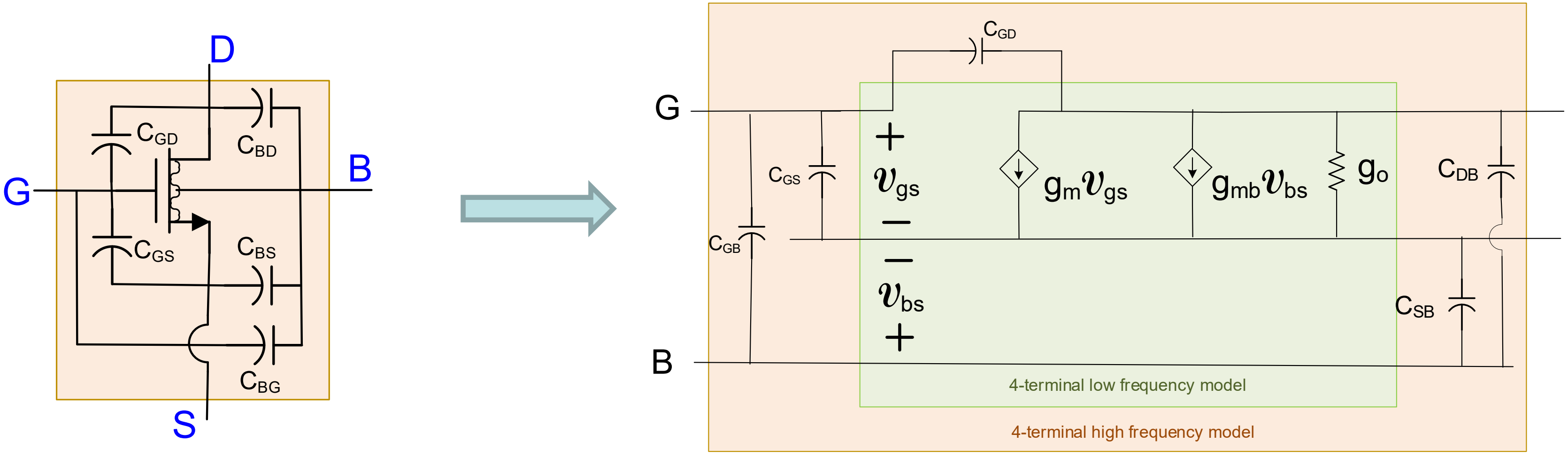
High Frequency Small Signal Model
(saturation region)

Often V_{BS}=0 and C_{BG}=0 in saturation, so simplifies to

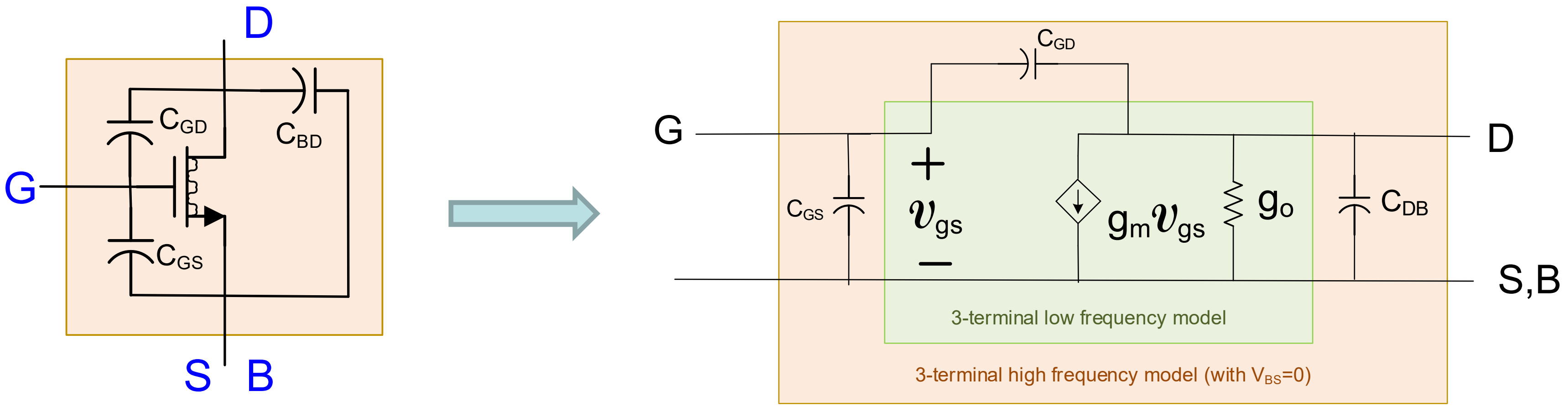


High Frequency Small-Signal Model

(Saturation Region)

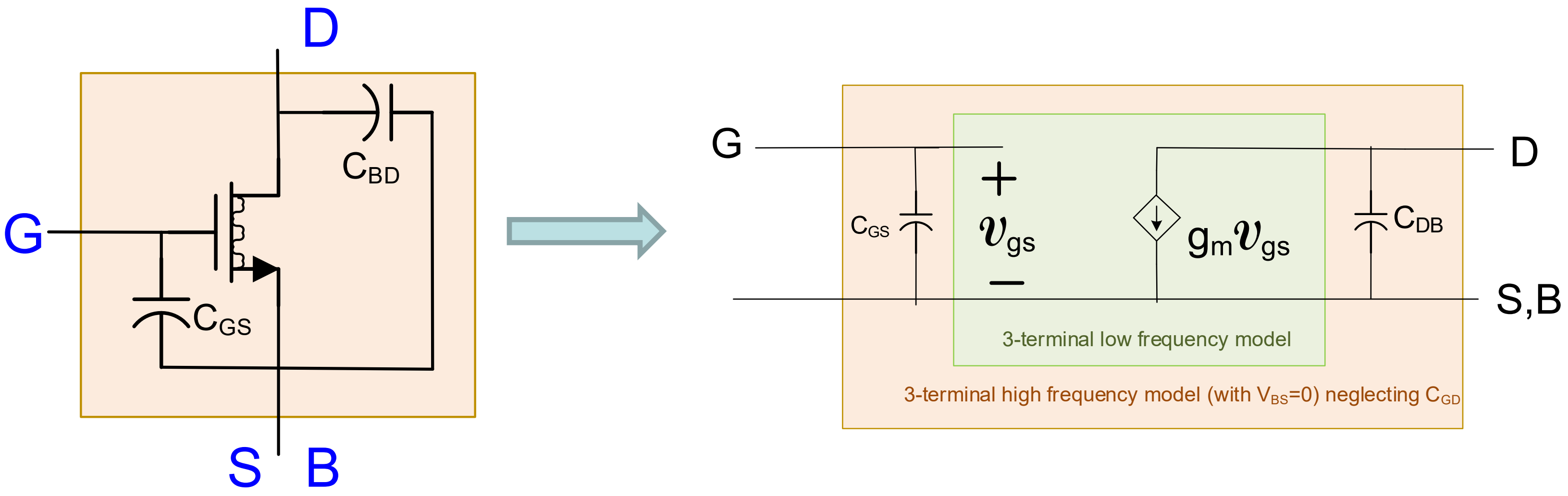


Often $V_{BS}=0$ and $C_{BG}=0$, so simplifies to



High Frequency Small-Signal Model

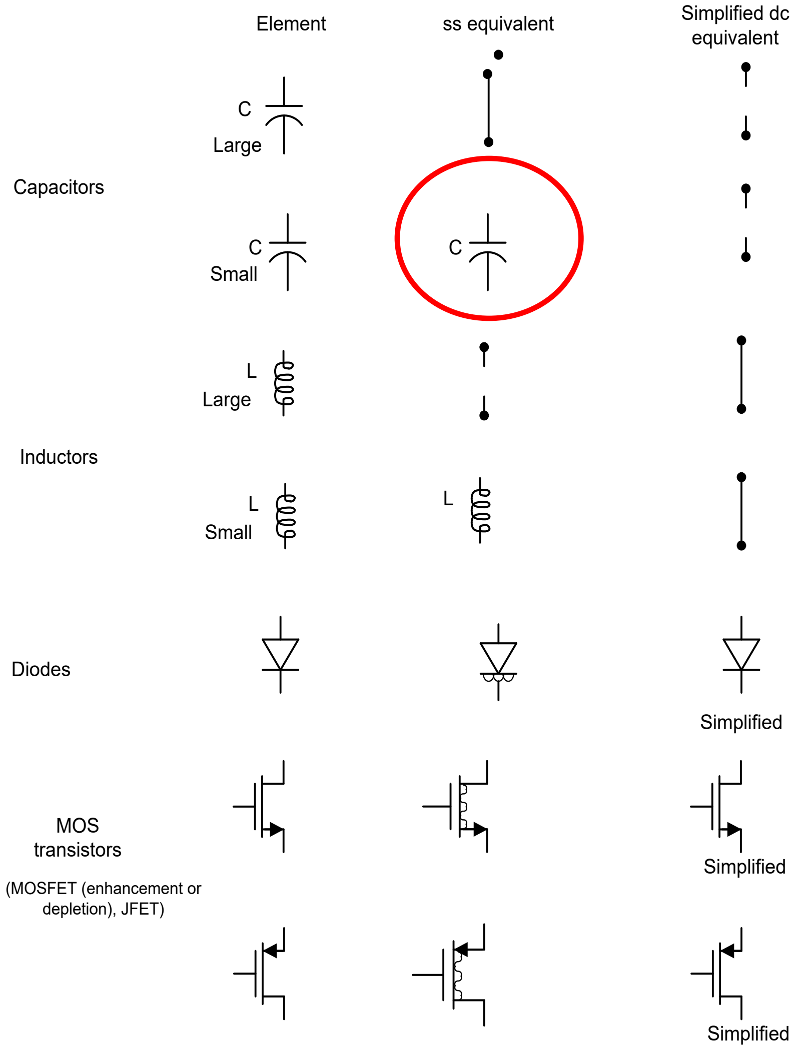
Often V_{BS}=0 and C_{BG}=0 and C_{GD} and g_0 can be neglected so simplifies farther to



Neglecting C_{GD} which is high frequency feedback from output to input often simplifies analysis considerably

Recall:

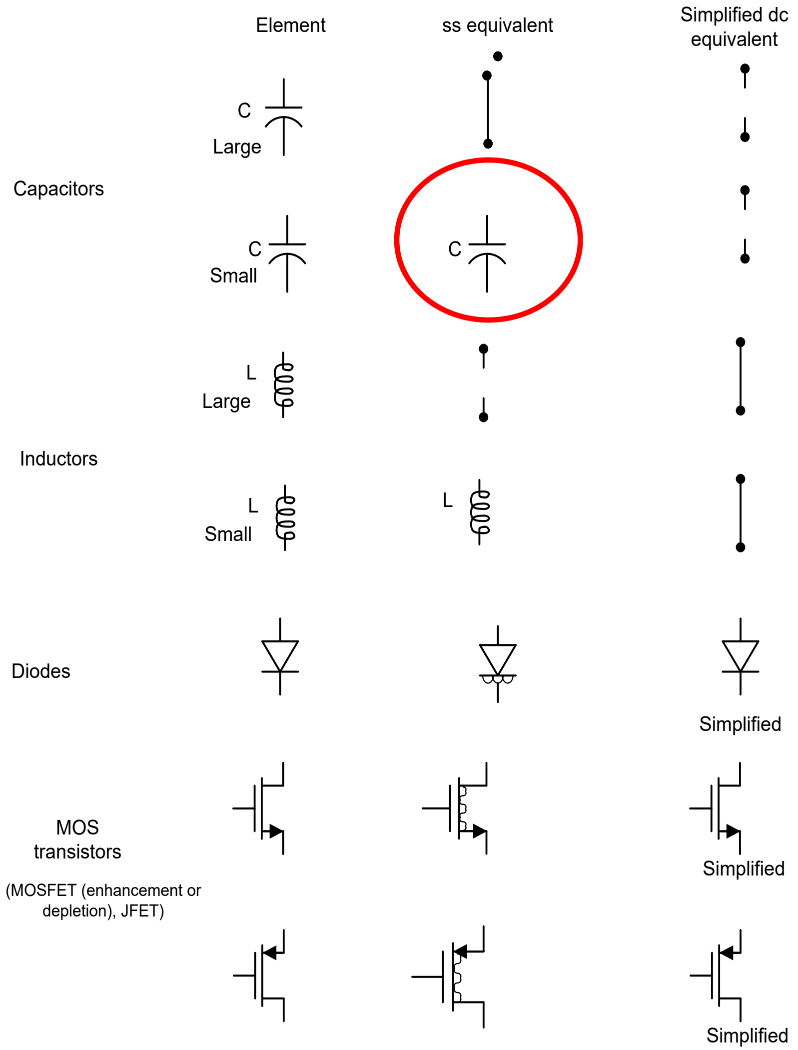
Small-signal and simplified dc equivalent elements



Have not yet considered situations where the small capacitor is relevant in small-signal analysis

Recall:

Small-signal and simplified dc equivalent elements

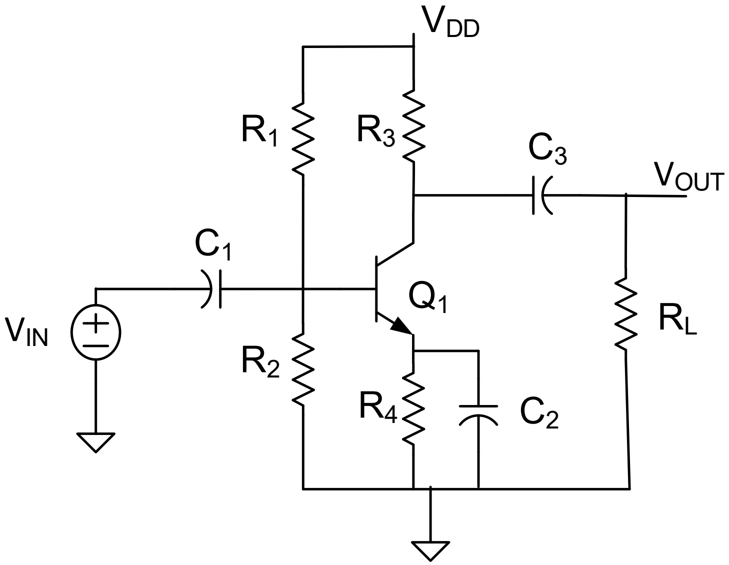


Have not yet considered situations where the small capacitor is relevant in small-signal analysis

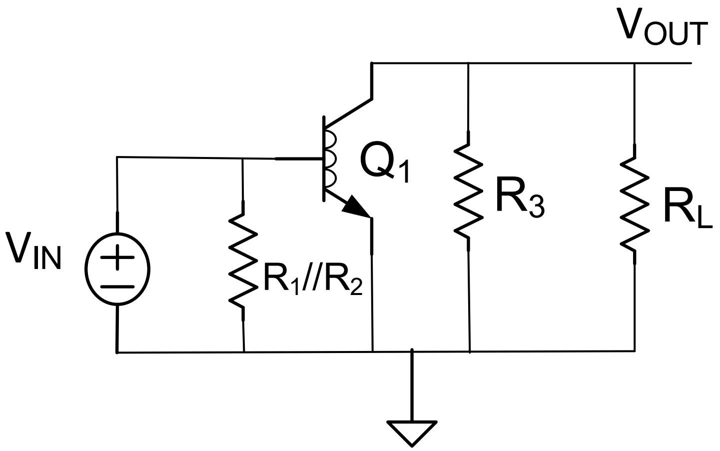
Amplifiers with Small Capacitors

Consider a bipolar amplifier first where C_3 is a small capacitor but not a parasitic capacitor

Recall:



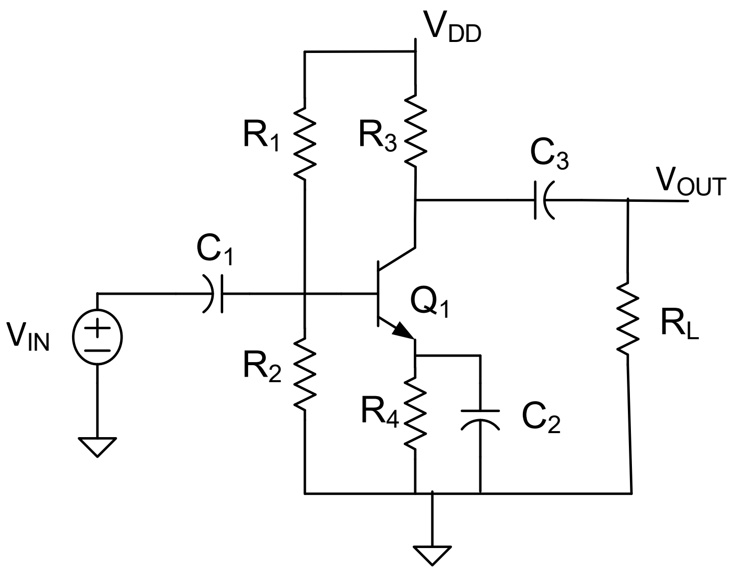
If capacitors are large

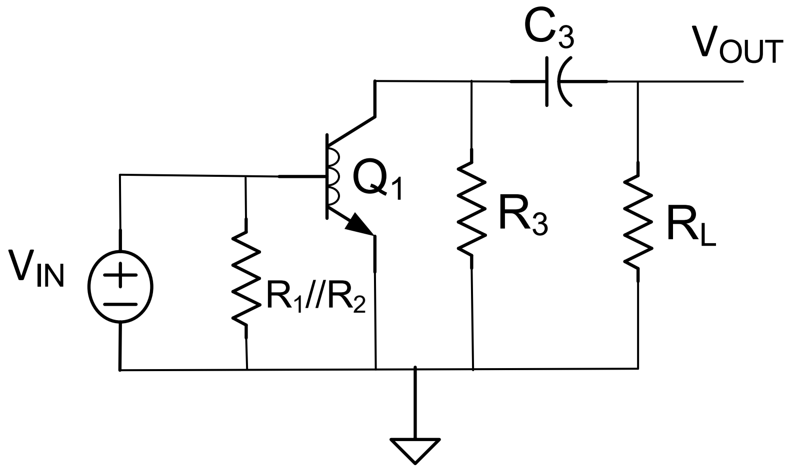


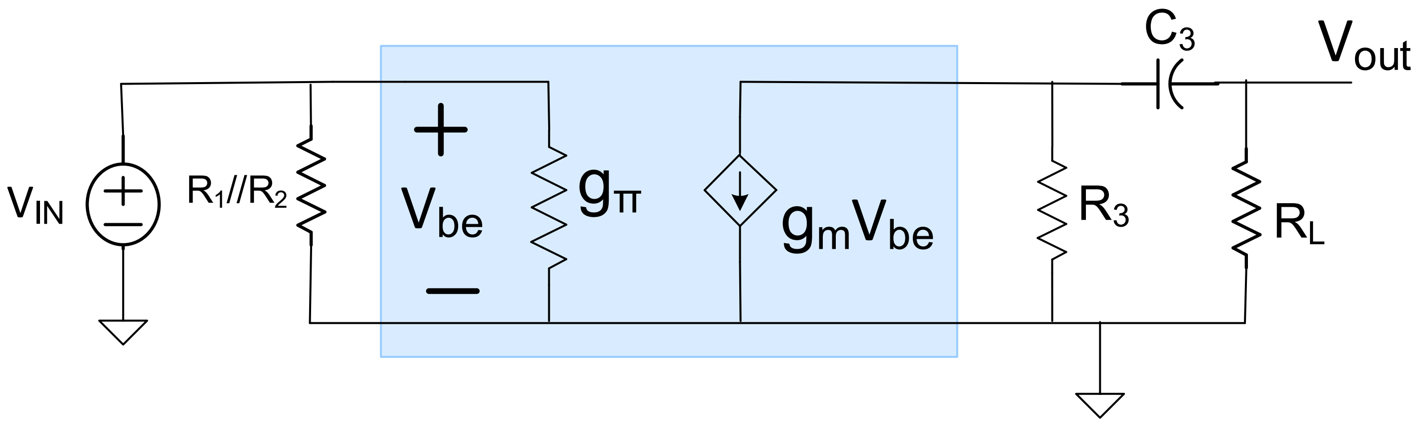
$$A_V = -g_{m1} \bullet R_3 // R_L$$

Amplifiers with Small Capacitors

What if C_1 and C_2 large but C_3 is not large?:

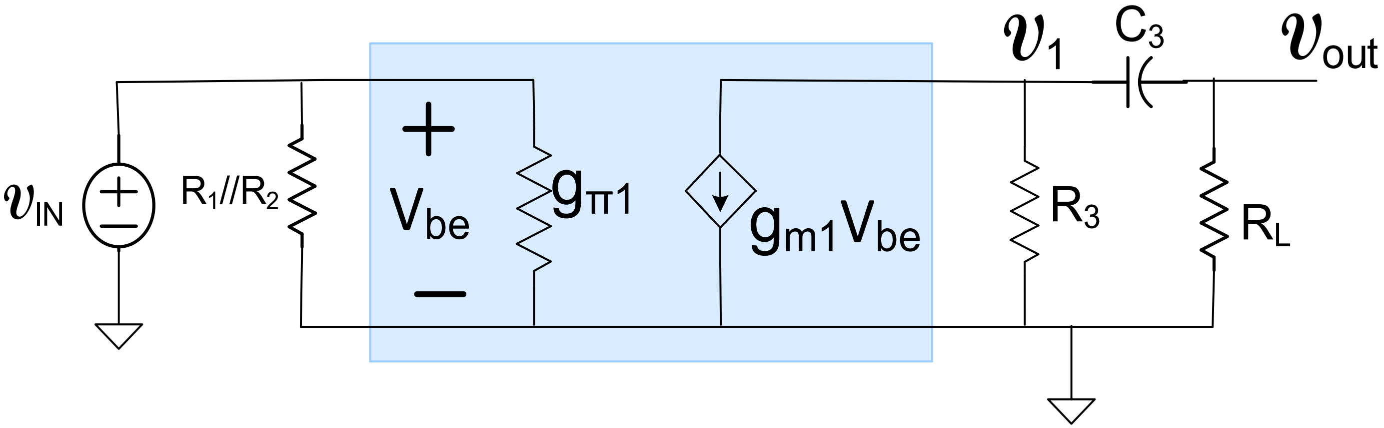






Amplifiers with Small Capacitors

What if C_1 and C_2 large but C_3 not large?:



From KCL:

$$\left.\begin{aligned} v_{OUT}\left(sC_3+G_L\right) &= v_1 sC_3 \\ v_1\left(sC_3+G_3\right)+g_{m1}v_{IN} &= v_{OUT}sC_3 \end{aligned}\right\}$$

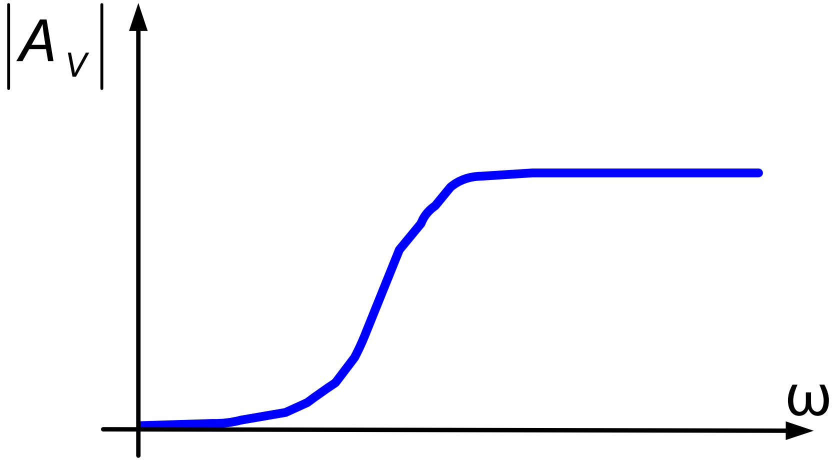
Solving:

$$\frac{v_{OUT}}{v_{IN}} = -\frac{-sC_3 g_{m1}}{sC_3\left(G_L+G_3\right)+G_3G_L}$$

Equivalently:

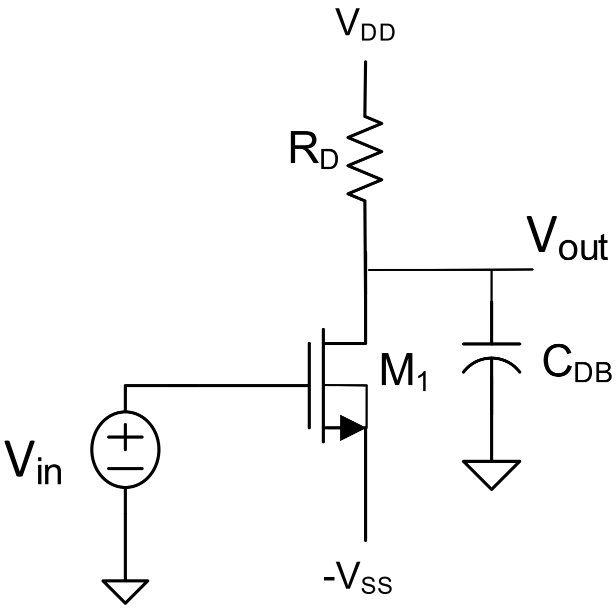
$$\frac{v_{OUT}}{v_{IN}} = -\frac{g_{m1}sC_3R_3R_L}{sC_3\left(R_L+R_3\right)+1}$$

Serves as a first-order high-pass filter

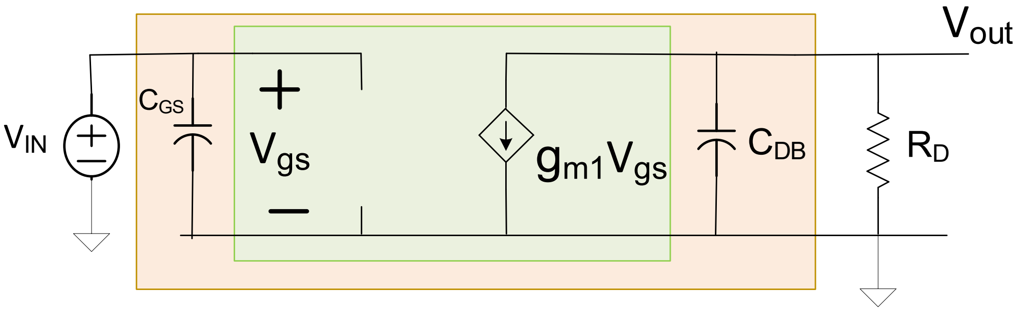


Amplifiers with Small Capacitors

Consider parasitic C_{GS} and C_{DB}



(this circuit is different from previous)



By KCL:

$$v_{OUT}\left(sC_{DB}+G_D\right)=-g_{m1}v_{IN}$$

Solving:

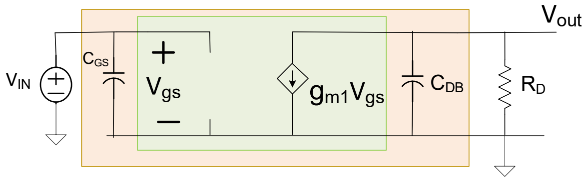
$$\frac{v_{OUT}}{v_{IN}}=-\frac{g_{m1}}{sC_{DB}+G_D}$$

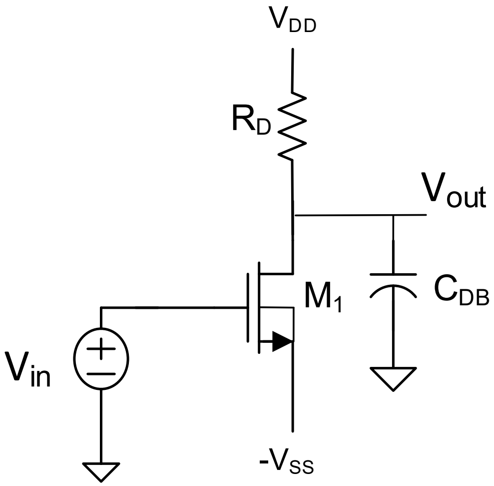
Equivalently:

$$\frac{v_{OUT}}{v_{IN}}=\frac{-g_{m1}R_D}{sC_{DB}R_D+1}$$

Amplifiers with Small Capacitors

Consider parasitic C_{GS} and C_{DB}



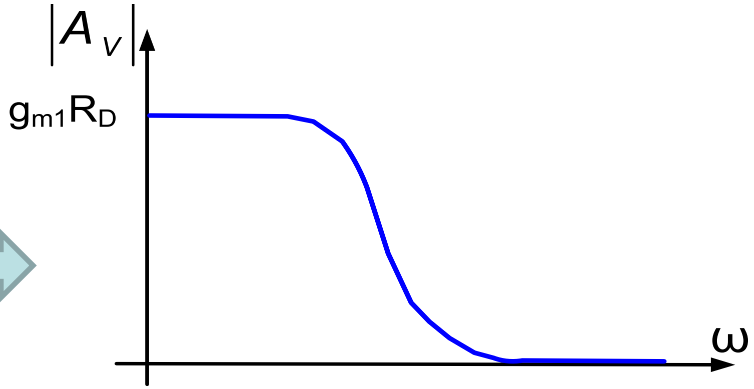


$$\frac{v_{OUT}}{v_{IN}} = A_V(s) = -\frac{g_{m1}R_D}{sC_{DB}R_D + 1}$$

$$A_V(j\omega) = \frac{-g_{m1}R_D}{j\omega C_{DB}R_D + 1}$$

$$\left|A_V(j\omega)\right| = \frac{g_{m1}R_D}{\sqrt{\left(\omega C_{DB}R_D\right)^2 + 1}}$$

$$\angle A_V(j\omega) = -180^o - \tan^{-1}\left(\frac{\omega C_{DB}R_D}{1}\right)$$

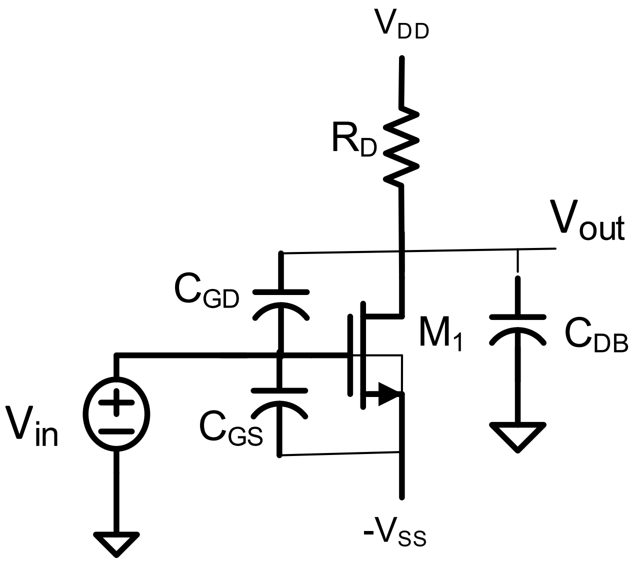


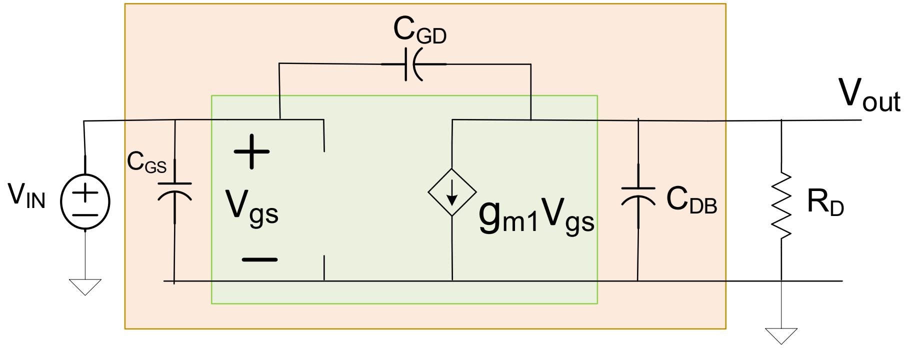
Since first-order low-pass, half-power frequency given by

$$\omega_{3dB} = \frac{1}{R_D C_{DB}}$$

Amplifiers with Small Capacitors

Consider parasitic C_{GS}, C_{GD}, and C_{DB}





By KCL:

$$v_{OUT}\left(s\left[C_{DB}+C_{GD}\right]+G_D\right)=-g_{m1}v_{IN}+sC_{GD}v_{IN}$$

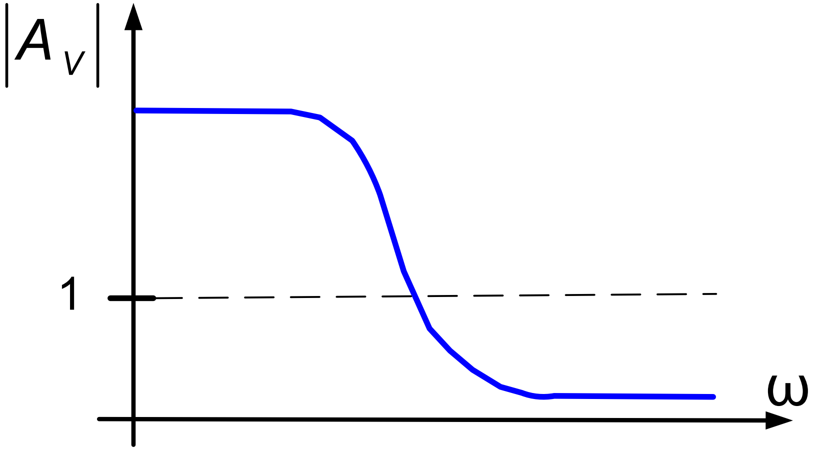
C_{DB} causes gain to decrease at high frequencies
C_{GD} causes feed-forward and limits high frequency drop
Has one LHP pole and one RHP zero

Solving:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}+sC_{GD}}{s\left[C_{DB}+C_{GD}\right]+G_D}$$

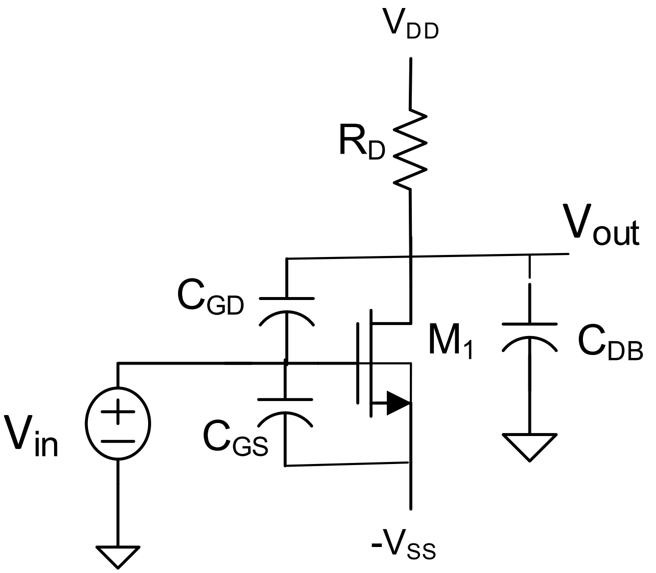
Equivalently:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-R_D\left(g_{m1}-sC_{GD}\right)}{s\left[C_{DB}+C_{GD}\right]R_D+1}$$



Amplifiers with Small Capacitors

Consider parasitic C_{GS}, C_{GD}, and C_{DB}



Device parasitics problematic at high frequencies

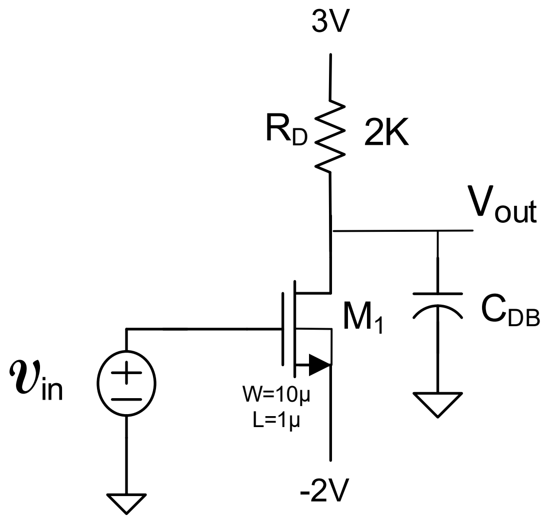
C_{DB}, C_{GD} and C_{GS} effects can be significant

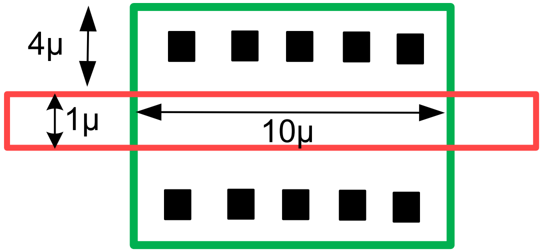
Value of parasitic capacitances strongly dependent upon layout

Device parasitics usually not a problem at audio frequencies

Causes gain to decrease at high frequencies:
has one high frequency LHP pole and one high frequency RHP zero.

Example: Determine the small-signal voltage gain and the 3dB bandwidth. Consider only the effects of C_{DB} on the BW. Assume a 0.5u process with V_{TH}=0.75V and the layout of the transistor shown.





$C_{DB}=C_{BOT}*40u^2+C_{SW}*28u$

$C_{BOT}=942aF/u^2 \quad C_{SW}=212aF/u$

From PDK

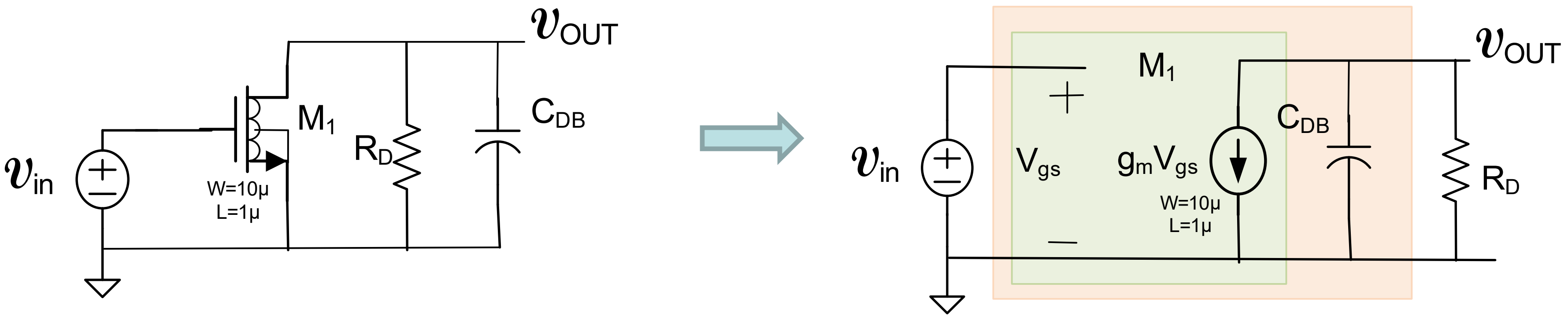
$C_{DB}=942aF/u^2*40u^2+212aF/u*28u$

$C_{DB}=37.7fF+5.9fF=43.6fF$

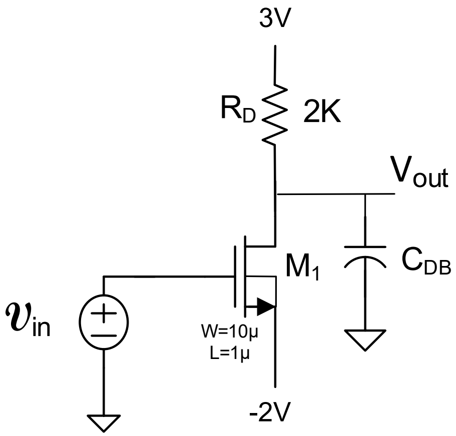
Solution:

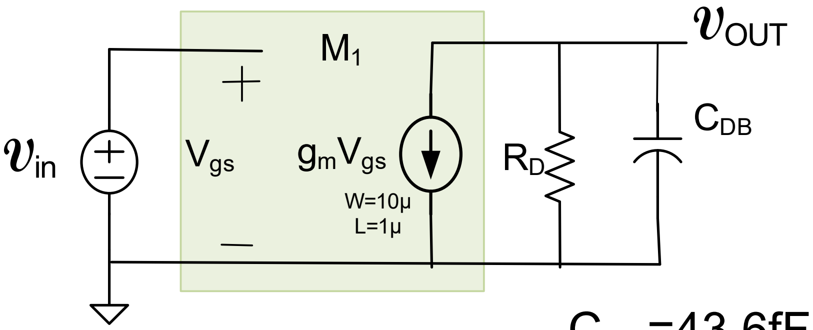
$$I_{DQ}=100\mu A/V^2\frac{10}{2\bullet 1}(2-0.75)^2=0.78mA$$

$$I_{DQ}R_D=0.78mA\bullet 2K=1.56$$



Example: Determine the small-signal dc voltage gain and the 3dB bandwidth. Consider only the effects of C_{DB} on the BW. Assume a 0.5u process with V_{TH}=0.75V and the layout of the transistor shown.



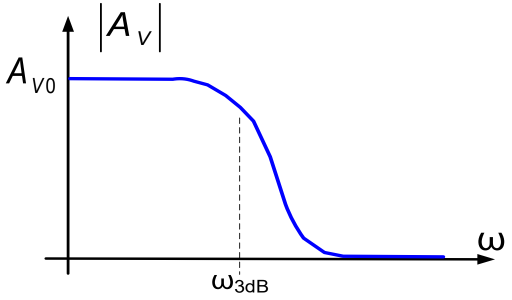


C_{DB}=43.6fF

Solution continued:

$$v_{OUT}\left(G_D + sC_{DB}\right) + g_m v_{IN} = 0$$

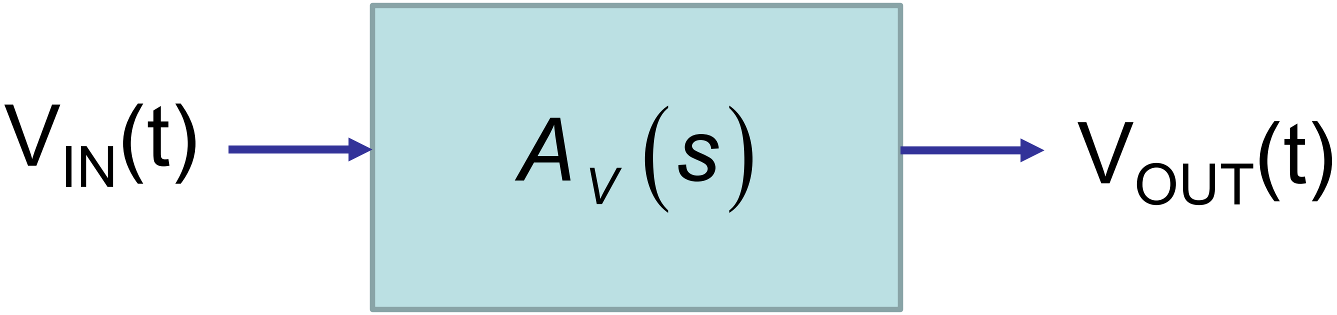
$$v_{OUT} = -v_{IN}\frac{g_m R_D}{1+sC_{DB}R_D}$$



$$A_{V0} = -g_m R_D = -\frac{2I_{DQ}R_D}{V_{EB}} = -\frac{3.12}{1.25} = -2.5$$

$$f_{3dB} = \frac{1}{2\pi} \bullet \frac{1}{R_D C_{DB}} = 1.8GHz$$

Sinusoidal Steady State Response for Linear Systems


$V_{IN}(t)$

$A_V(s)$

$V_{OUT}(t)$

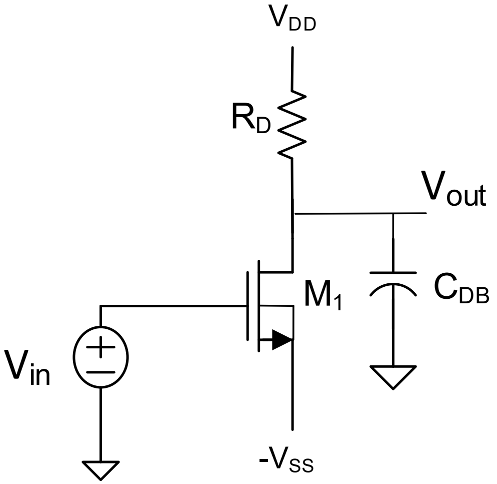
Key Result from EE 201

If $V_{IN}=V_m\sin(\omega t+\theta)$ where V_m is small (so linear operation maintained)

Steady state output is also a sinusoid given by

$$V_{OUT}(t)=V_m\left|A_V(j\omega)\right|\sin\left(\omega t+\theta+\angle A_V(j\omega)\right)$$

Sinusoidal Steady State Response for Linear Systems



$$\left|A_V(j\omega)\right| = \frac{g_{m1}R_D}{\sqrt{\left(\omega C_{DB}R_D\right)^2+1}}$$

$$\angle A_V(j\omega) = -180^o - \tan^{-1}\left(\frac{\omega C_{DB}R_D}{1}\right)$$

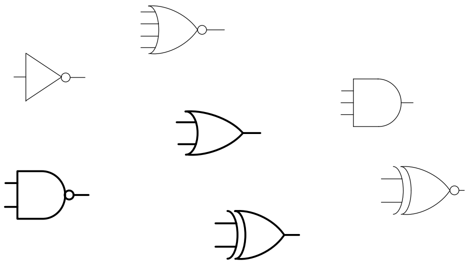
If $V_{IN}=V_m\sin(\omega t+\theta)$

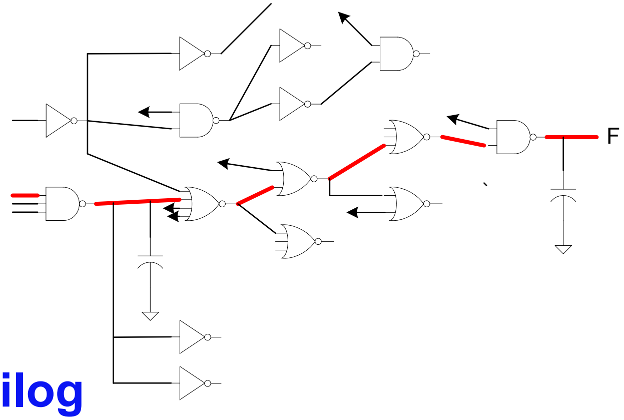
For V_m small, small-signal steady state output given by

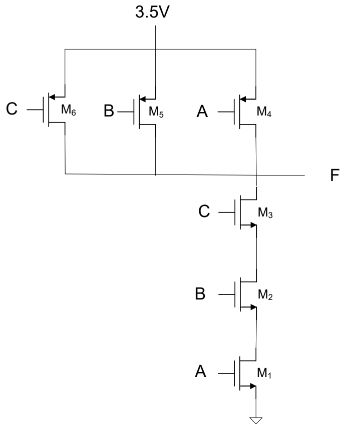
$$V_{OUT}(t) = V_m \frac{g_{m1}R_D}{\sqrt{\left(\omega C_{DB}R_D\right)^2+1}}\sin\left(\omega t+\theta-180^o-\tan^{-1}\left(\frac{\omega C_{DB}R_D}{1}\right)\right)$$

Digital Circuit Design

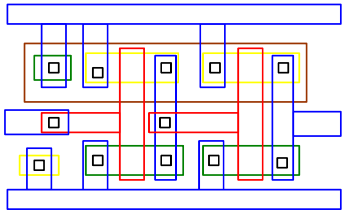
Most of the remainder of the course will be devoted to digital circuit design







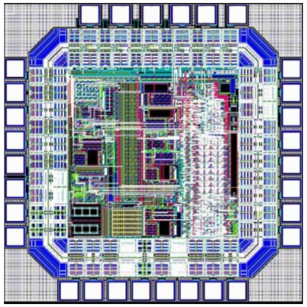
Verilog

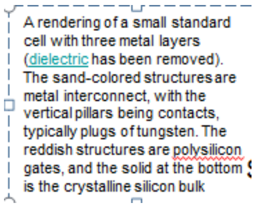


```
module gates (input logic [3:0] a,b,
             output logic [3:0] y1,y2,y3,y4,y5);
  assign y1 = a&b;  //AND
  assign y2 = a | b;  //OR
  assign y3 = a ^ b;  //XOR
  assign y4 = ~(a & b);  //NAND
  assign y5 = ~( a | b);  //NOR
endmodule
```

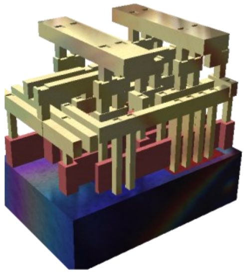
VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity gates is
   port(a,b: in STD_LOGIC_VECTOR(3 dowto 0);
            y1,y2,y3,y4,y5:out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture synth of gates is
begin

y1 <= a and b;
y2 <= a or b;
y3 <= a xor b;
y4 <= a nand b;
y5 <= a nor b;
end;
```





A rendering of a small standard cell with three metal layers (dielectric has been removed). The sand-colored structures are metal interconnect, with the vertical pillars being contacts, typically plugs of tungsten. The reddish structures are polysilicon gates, and the solid at the bottom is the crystalline silicon bulk

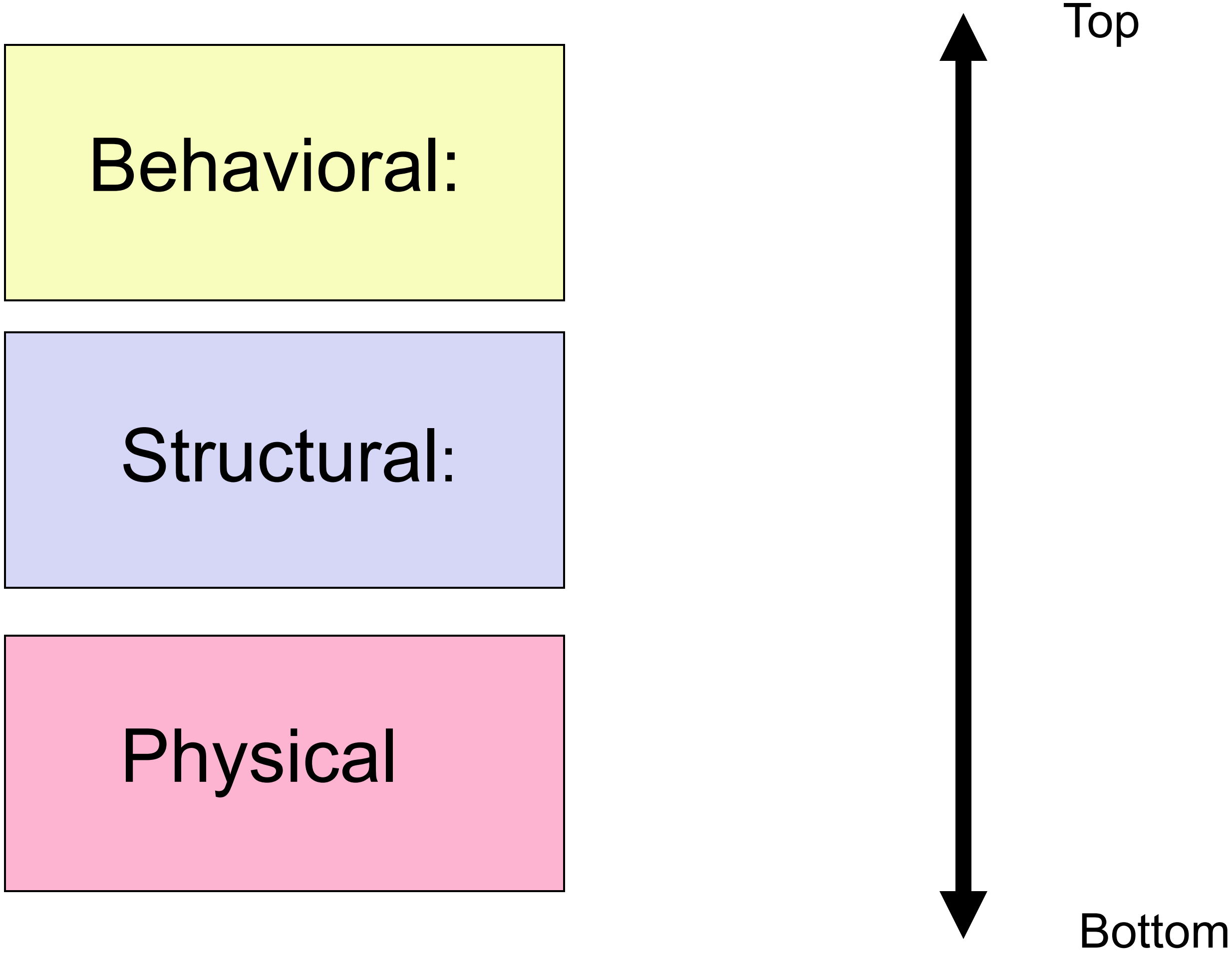


Standard Cell Library

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

Hierarchical Digital Design Domains:



Top

Behavioral:

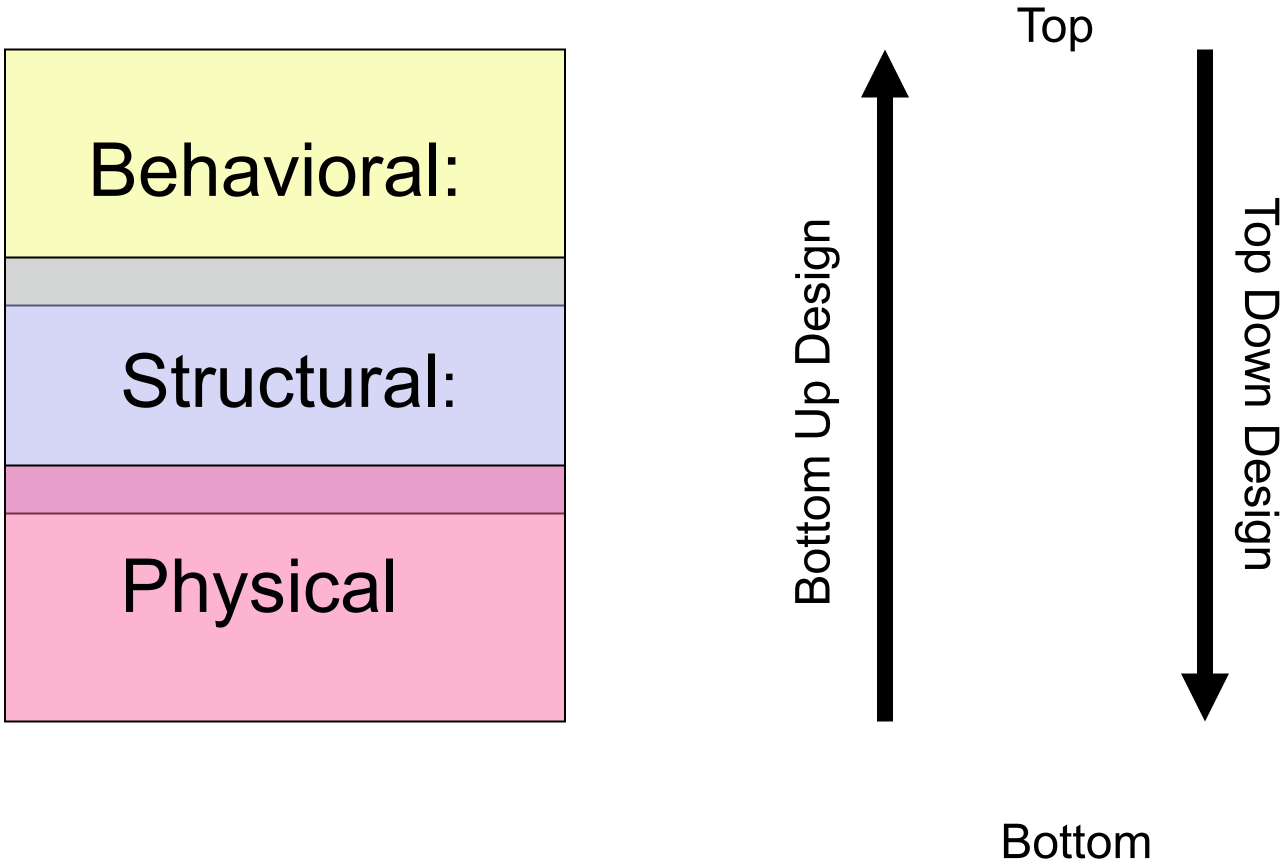
Structural:

Physical

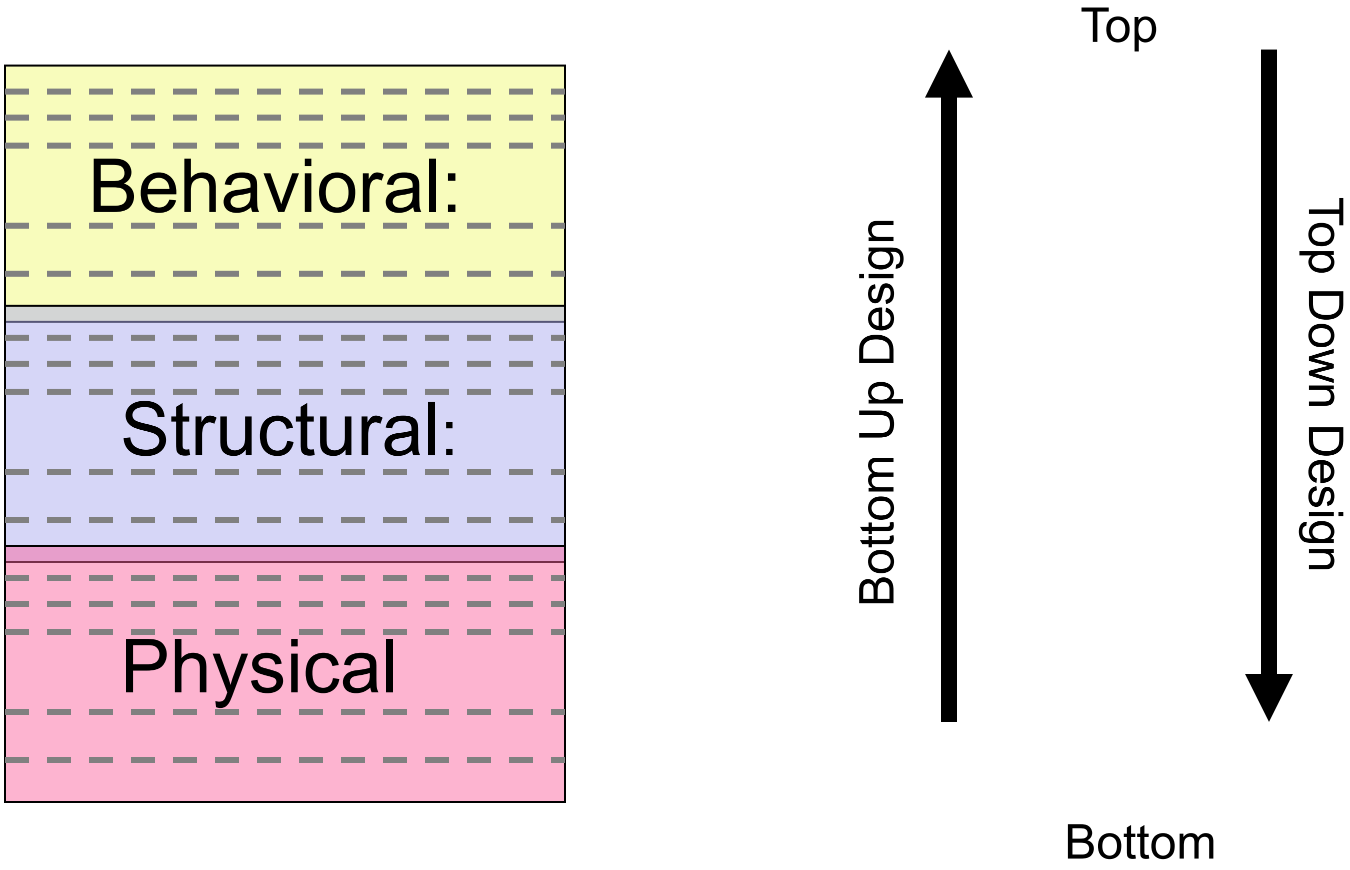
Bottom

Multiple Levels of Abstraction

Hierarchical Digital Design Domains:



Hierarchical Digital Design Domains:



Behavioral:

Structural:

Physical

Top

Bottom Up Design

Top Down Design

Bottom

Multiple Sublevels in Each Major Level

All Design Steps may not Fit Naturally in this Description

Hierarchical Digital Design Domains:

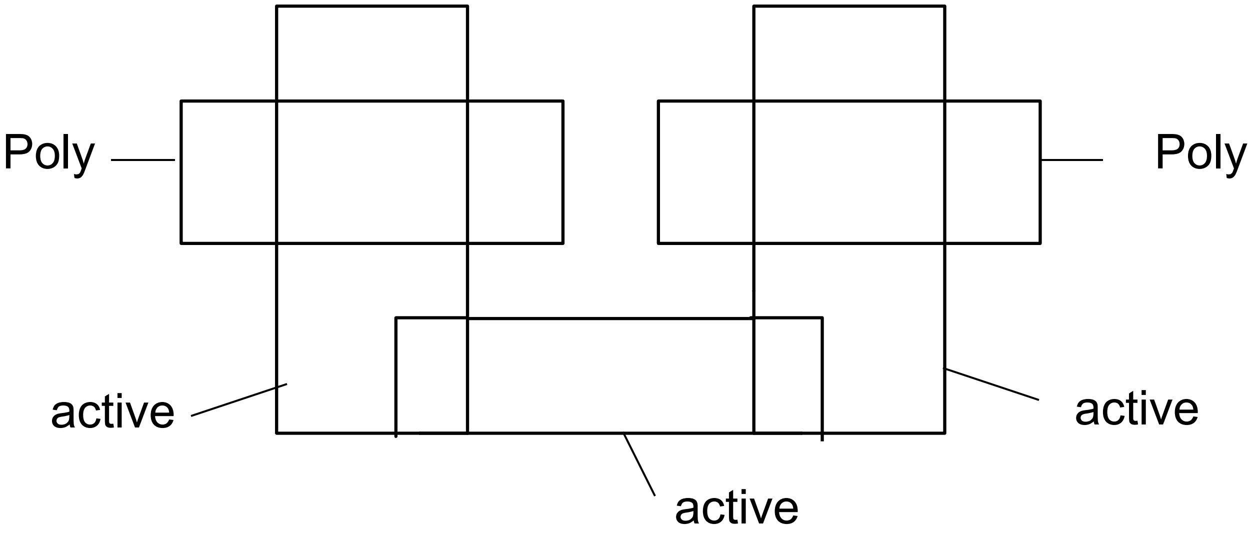
Behavioral : Describes what a system does or what it should do

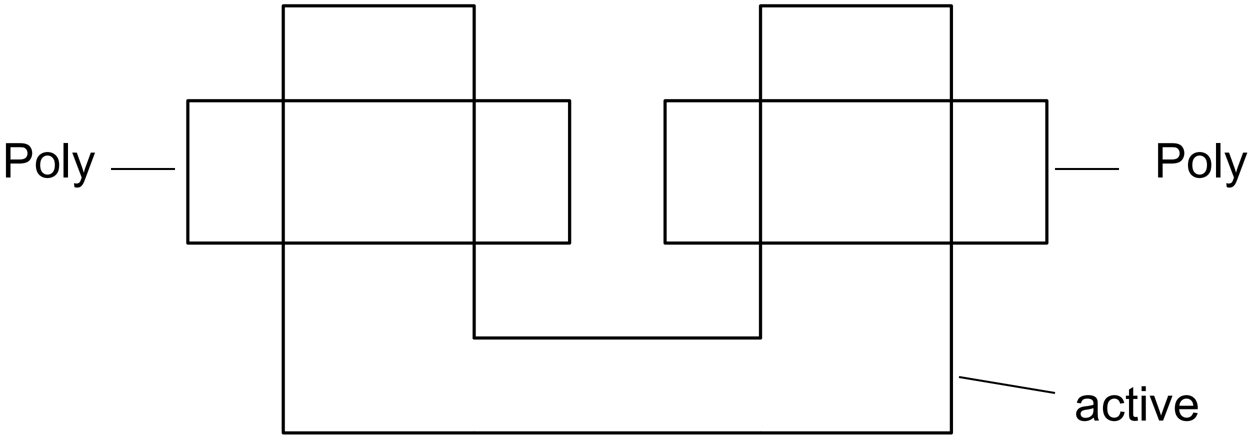
Structural : Identifies constituent blocks and describes how these blocks are interconnected and how they interact

Physical : Describes the constituent blocks to both the transistor and polygon level and their physical placement and interconnection

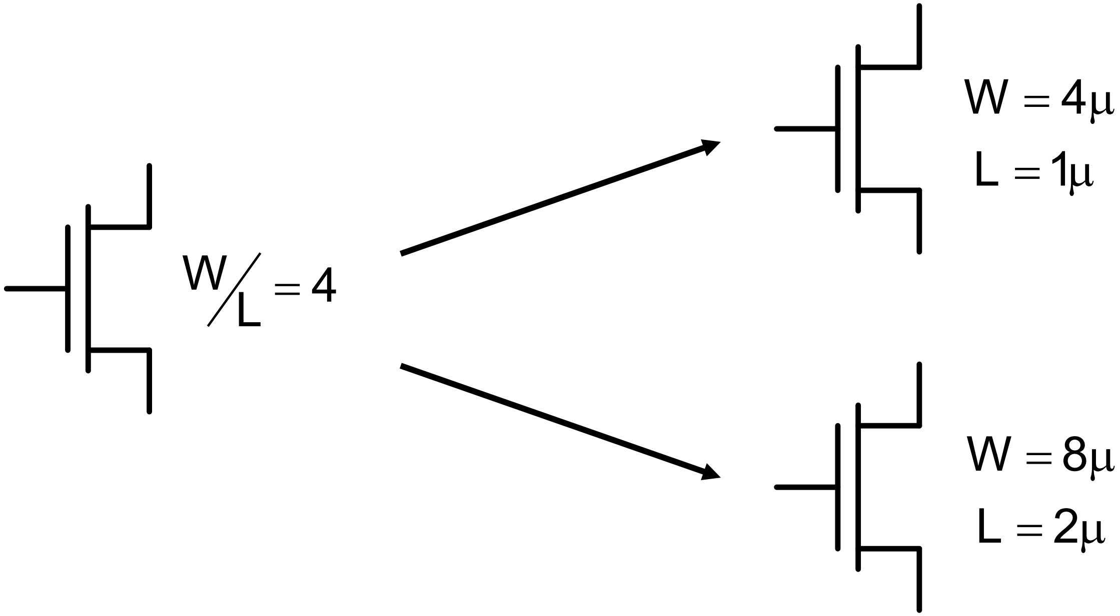
Multiple representations often exist at any level or sublevel

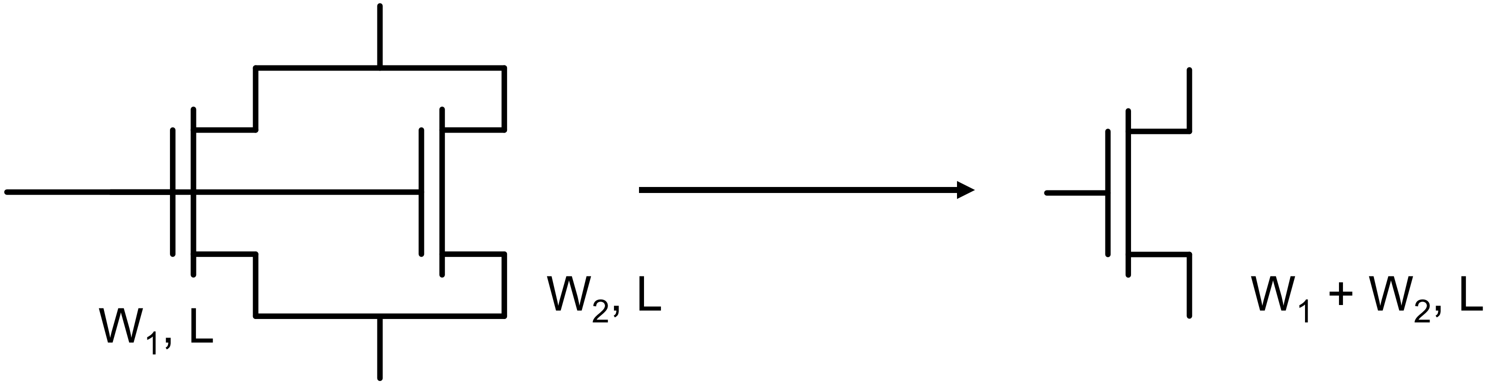
Example: Two distinct representations at the physical level (polygon sublevel)



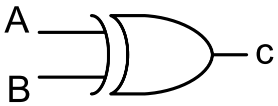


Example: Two distinct representations at physical level (schematic sublevel)

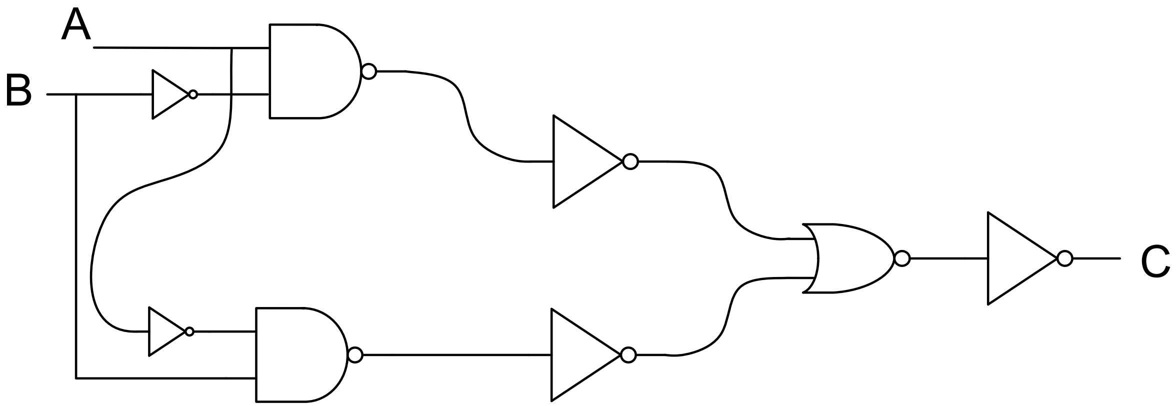


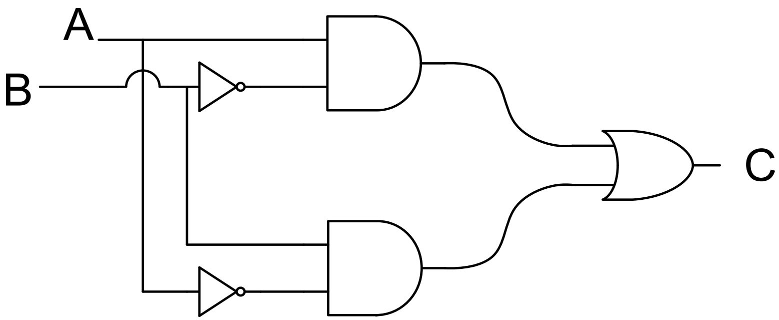


Example: Three distinct representations at the structural/behavioral level (gate sublevel)



$$C = A \oplus B$$





In each domain, multiple levels of abstraction are generally used.

Consider Physical Domain

- Consider lowest level to highest

0 - placement of diffusions, thin oxide regions, field oxide, ect. on a substrate.

1 - polygons identify all mask information (not unique)

2 - transistors (not unique)

3 - gate level (not unique)

4 - cell level

Adders, Flip Flop, MUTs,…

Information Type

PG data
G.D.F
Netlist
HDL Description

Structural Domain:

- DSP
- Blocks (Adders, Memory, Registers, etc.
- Gates
- Transistor

Information Type

HDL

Netlists

Behavior Domain (top down):

- Application
- Programs
- Subroutines
- Boolean Expressions

Information Type

High-Level Language
HDL

Representation of Digital Systems

Standard Approach to Digital Circuit Design

8 – level representation

1. Behavioral Description
   - Technology independent
2. RTL Description (Register Transfer Level)

   (must verify (1) ⇔ (2))
3. RTL Compiler

   Registers and Combinational Logic Functions
4. Logic Optimizer
5. Logic Synthesis

   Generally use a standard call library for synthesis

(sublevels 6-8 not shown on this slide)

Frontend design

Representation of Digital Systems

Standard Approach to Digital Circuit Design

1. Behavioral Description
    - Technology independent
2. RTL Description

    (must verify (1) ⇔ (2))
3. RTL Compiler

    Registers and Combinational Logic Functions
4. Logic Optimizer
5. **Logic Synthesis**

    Generally use a standard call library for synthesis

HDL

Backend design

6. Place and Route

   (physically locates all gates and registers and interconnects them)

7. Layout Extraction
   - DRC
   - Back Annotation

8. Post Layout simulation

   May necessitate a return to a higher level in the design flow

Logic synthesis, though extensively used, often is not as efficient nor as optimal for implementing some important blocks or some important functions

These applications generally involve transistor level logic circuit design that may combine one or more different logic design styles

End of Lecture 36